BIO-DATA

Name **: DR. JATINDRA NATH ROY**

Date of Birth **:** 12th June 1957

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Academic Qualifications:

Ph.D in Materials Science: Sept. 1980 to Jan 1984 from IIT-Kharagpur.
D.I.I.T in Industrial Physics: 1980 from IIT- Kharagpur
M.Sc. (Physics): 1979 from IIT – Kharagpur

Professional Profile:

Since March 2014:
Visiting Professor (ATDC & SESE) : IIT-Kharagpur
Joint faculty in ATDC (Advance Technology Development Centre) and SESE (School of Energy Science & Engineering). ATDC is engaged in multi-disciplinary research in the area of Microelectronics, MEMS and other related Materials and Devices. SESE is a new initiative of IIT-Kharagpur in the area of Energy, including Renewable Energy such as Solar PV. I have been instrumental to start research programs, including Ph. D., and a PG Course (M. Tech in Energy).

July 2008 to Feb 2014:
Senior Vice President (R&D/Engineering/Quality/Reliability): Solar Semiconductor-Hyderabad. Solar Semiconductor is a Photo-Voltaic (PV) Company engaged in Cell & Module manufacturing and PV Systems for off-grid/Grid Interactive & Utility Scale power plants. I was a part of Senior Management team and responsible for R&D, Engineering,

Technology, Quality, Certification and Reliability related activities of the entire organization. I was a key player for setting up a state of the art facility located at Fab City for Cell and Module Manufacturing equipped with full-fledged Reliability Lab.

September 2006 to July 2008:
During this period, I was with **Semi-Conductor Laboratory (SCL), previously known as Semiconductor Complex Limited (SCL), as Scientist/Engineer: "G".** I was responsible for complete VLSI operation (Process Technology Development, VLSI design, VLSI & MEMS Manufacturing, Testing and Assembly). I was part of the core team engaged in an upgradation plan with total financial outlay of about $250M. The details were worked out, vendor selection was done and a draft agreement finalized.

October 2004 to September 2006:
I was **Professor (Microelectronics) under "Faculty of Engineering" in Panjab University-Chandigarh** during this period. I was course co-ordinator for M.Tech (Microelectronics) and M.Tech (Nanoscience & Nanotechnology) courses. I was involved in teaching and research in the area of IC fabrication, Device modeling, Circuit simulation & modeling, Analog & Mixed Signal design and Nanoelectronics.

January 1884 to October 2004:
This was my first employment immediately after completing Ph.D. I was with **Semiconductor Complex Limited (SCL); joined as Senior Engineer (R&D) and was General Manager (R&D and Design) when left.** I was a part of Senior Management team and a key member of a team responsible for setting up a 6 inch VLSI facility including wafer fabrication, Design, assembly, test and QA/QC with an investment of about $100M.
I was responsible for the development of several high end technologies, such as CMOS, EEPROM, High Voltage CMOS, Rad Hard, CCD, MEMS, etc. I was also responsible for the development of special products such as CCD imagers, ASICs as well as several standard products. I had worked in reputed foreign foundries and have joint collaboration projects with several organizations in India and abroad.

Membership/Reccognition/Award

Fellow: Indian National Academy of Engineering (FNAE)
Distinguished Visiting Professor: INAE
Member of INAE Sectional Committee
Senior Member: IEEE (SMIEEE)
Fellow-IMS (Indian Microelectronics Society)
Secretary for three consecutive years of IMS
Honorary Chair of IEEE Chandigarh Sub-section
Honorary Vice Chair of IEEE Hyderabad Section
Best innovator award from EDN-Asia in Nov 1996
Consultant (2005-2006) to Analog Integration Corporation (AIC) – USA
Expert committee member of CDN Live 2006 & 2007 of Cadence.
Conducted Corporate Training for Cypress- India and Cypress-Philippines
Key member of organizing team for several conferences/workshops including Five IMS

Conferences
Guest faculty for various reputed Institutions
Part of Scientific Committee: EUPVSEC-2012 (Frankfurt, Germany) and EUPVSEC-2013 (Paris, France) and EUPVSEC-2015 (Hamburg, Germany)

BOOK

1. **J.N.Roy** and D.K.Syal: Editor of "Trends in VLSI and Embedded Systems": Macmillan Advanced Research Series: 2007
2. **J.N.Roy** and D.N.Bose: Introduction to VLSI Design and Technology: New Age International Publishers, 2010.

PUBLICATIONS:

1. **J.N.Roy,** S.Basu and D.N.Bose: Low Temperature Growth of Poly Crystalline Indium Phosphide; Solar Energy Materials 5(4), 379, (1981).
2. **J.N.Roy,** S.Basu and D.N.Bose: Grain Size Dependence of Mobility in Poly Crystalline n-Indium Phosphide: Journal of Applied Physics 54 (2), 395, (1983).
3. **J.N.Roy,** S.Basu, D.N.Bose and A.J.Singh: Behavior of Large Grain Polycrystalline n-indium Phosphide Grown by SSD Technique: Indian Journal of Pure and Applied Physics 21(70) 395(1983).
4. D.N.Bose, **J.N.Roy** and S.Basu: Improved Schottky Barrier Height on n-Indium Phosphide by Surface Modification: Materials Letters 5B, 455, (1984).
5. **J.N.Roy,** Harish K. Chaudhury and M.J.Zarabi: Effects of Field Implants on Small Geometry CMOS devices: Microelectronics and Reliability 27(6), 953, (1987).
6. **J.N.Roy,** H.C.Mohanty, Bharat Bhushan, M.V.R.Yogi, P.A.Govindacharyulu, D.N.Singh and M.J.Zarabi: Development of 2μm CMOS Process: Electronics Today, Aug 1988.
7. **J.N.Roy,** S.Basu and D.N.Bose: Characterisation of Grain Boundary in Polycrystalline n-InP Grown by Gradient-Freeze Method: Materials Letters 7, 359, (1989)
8. **J.N.Roy:** Bulk Growth of Polycrystalline Indium Phosphide: Bulletin of Materials Sciences 13(1), 3(1990).
9. **J.N.Roy,** S.Basu and D.N.Bose: Characterization of n-InP Crystals Grown by Gradient Freeze Method of Different Phosphorus Vapour Pressures: Indian Journal of Pure and Applied Physics 29, 555, (1991).
10. **J.N.Roy** and M.J.Zarabi: Materials for VLSI Processes: IETE Journal of Research: Special Issue on Materials for Electronics: 43 (2&3), March-June 1997, PP 207-213.
11. D.K.Pal, S.M.Pandey, H.Jain and **J.N.Roy:** Model for Metal Interconnection Design Rule Optimization: Microelectronics Engineering 56(2001) 295-302.
12. **J.N.Roy,** S.Basu and D.N.Bose: Growth of Indium Phosphide and Application in PEC Solar Cells: Proceedings of "International Workshop on the Properties of the Physics of Semiconductor devices", Held at Indian Institute of Technology-Delhi (India), Nov 1981.

13. Y. Ramprakash, **J.N.Roy**, S.Basu and D.N.Bose: n-PEC Solar Cells in Presence of Ruthenium Ions: Proceedings of "Solar Energy congress, International Solar energy Society", Held at Perth (Australia) 1983.
14. **J.N.Roy,** S.Basu and D.N.Bose: Grain Boundary Studies in n-Indium Phosphide: Proceedings of "International Symposium on Compound semiconductors and Related Technology", Held at Indian Institute of Technology-Madras (India), Sept. 1983.
15. **J.N.Roy,** S.Basu and D.N.Bose: Growth and Characterization of Indium Phosphide: Proceedings of "International Symposium on Compound Semiconductors and Related Technology", Held at Indian Institute of Technology-Madras (India), Sept.1983.
16. **J.N.Roy and M.J.Zarabi:** Characterization of Ion Implanted Silicon-A Review: Proceedings of "International Symposium of Semiconductor and Fibre Optics Communication", Held at CSIO, Chandigarh (India), Nov.1985.
17. S.Basu, **J.N.Roy** and D.N.Bose: Contact Behavior of Some Metals and Alloys on SSD Grown n-Indium Phosphide: Proceedings of "European Materials Research Society Conference", Held at Strasbourg (France), June 1986.
18. **J.N.Roy** and M.J.Zarabi: The Effect of Sub-threshold Conduction in Low Voltage Small Geometry CMOS Process: Proceedings of "International Symposium of Electronics Devices, Circuits and Systems", Held at IIT-Kharagpur (India) Dec. 87.
19. **J.N.Roy** and M.J.Zarabi: Control of Threshold Voltage and Body Factor of n-Channel Transistor Fabricated by Twin-tub CMOS Technology: National Conference on Electronic Circuits and Systems, Held at University of Roorkee (India), Nov 1989.
20. **J.N.Roy** and Rajesh Mehta: On Multilevel Metal Technology for 1.2µm CMOS Process: National Symposium on Advances in Microelectronic Devices and Fabrication Technology: Held at CSIO-Chandigarh (India) Nov.1992.
21. D.Dev and **J.N.Roy:** Fabrication of Oxide Sidewall Spacer for LDD structure: National Symposium on Advances in Microelectronic Devices and Fabrication Technique: Held at CSIO-Chandigarh (India): Nov 1992.
22. **J.N.Roy** and Vinod Chaku Optimization of Tub Design in Twin Tub Based CMOS Process: Proceedings of "International Workshop on Physics of Semiconductor Devices-93", Held at NPL-Delhi in Dec. 1993.
23. **J.N.Roy,** D.K.Datta, R.Rajagopal, Vinod Chaku and D.Dev: Contact Resistance Improvement by Barrier Metal and SALICIDE Technology: Proceedings of "International Workshop on Physics of Semiconductor Devices 93", Held at NPL-Delhi in Dec. 1993.
24. P.R.Verma**,** A. Bandyopadhyay and **J.N.Roy:** and High Voltage MOS Structures Compatible to Low Voltage CMOS process: Proceedings of "International workshop on Physics of Semiconductor Devices 95" Held at NPL-Delhi in Dec. 95.
25. Vinod Chaku, **J.N.Roy,** Krishna Kumar and Rajesh Goyal: Effect of Dielectric Layer on Top of Silicon surface on Responsivity of Different Photodiodes: Proceedings of "International workshop on Physics of Semiconductor Devices 95" Held at NPL-Delhi in Dec. 95.

26. G.K.Bhaumik, N.Ravi Kumar and **J.N.Roy:** Optimization of Reflection Loss of On-Chip Silicon Photodiode: Proceeding of "International Workshop on Physics of Semiconductor Devices" Held at Delhi, in Dec 97.
27. A.Datta, H.D. Banerjee and **J.N.Roy:** The Effect of TiN/$TiSi_2$ Bi-layer on Sheet and Contact Resistance in 1.2μm CMOS Technology: Proc. of "The International Conference on Computers and Devices for Communication (CODEC-98)", Held at Calcutta in 1998.
28. S.M.Pandey, H.Jain, D.K.Pal and **J.N.Roy:** Realization of Diffusion to Poly Capacitor in Salicide Based CMOS process: Proc. of "International Workshop on Physics of Semiconductor Devices" Held at New Delhi in Dec. 1999.
29. S.M.Pandey, N.Ravi Kumar, G.K.Sankar, D.K.Pal and **J.N.Roy:** Optimization of Dual Poly Gate Low Voltage CMOS Process: Proc. of "International Workshop on Physics of Semiconductor Devices" Held at New Delhi Dec. 1999.
30. N.Ravi Kumar, G.K.Sankar, **J.N.Roy** and D.N.Singh: Design and Realization of High performance CMOS Compatible Lateral Bipolar Transistors. (CLBTS). Proc. of "International Workshop on Physics of Semiconductor Devices" Held at New Delhi in Dec. 1999.
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39. D.K.Pal, H. Jain and **J.N.Roy:** Modeling of Current Carrying Capacity of Metal Interconnect: Chandigarh Synoposium on Microelectronics (CSME), Held at PU, Chandigarh, Feb.2001.

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41. Vivek Tripathi and **J.N.Roy:** Design of Sigma-Delta ADC: Chandigarh Synoposium on Microelectronics (CSME), Held at PU, Chandigarh, Feb.2001.
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47. **J.N.Roy:** Output Structure for Visible Imager Charge Coupled Devices: Invited Talk in VLSI Design and Test (VDAT) Conference-2003.
48. D.K.Routray, Deep Sehgal and **J.N.Roy:** Micropower Programmable Voltage Multiplier: Chandigarh Symposium on Microelectronics (CSME), Held at PU, Chandigarh, Feb.2003.
49. Deepak K. Syal and **J.N.Roy:** Embedded Systems and MEMS Structures for Tactile Displays: IMS Conference-2005, Held at Chandigarh in Feb,2005.
50. **J.N.Roy:** Nanoelectronics Device: Issues and Options: National Seminar on Information Technology-Recent Advances & Applications (ICT-2006), Held at JMIT-Radaur, Feb.2006
51. Rahul K. Singh and **J.N.Roy:** Modeling of N-Well device and N-well Field Resistor: Solid State Electronics : Vol 50, 1696-1704, 2006
52. Anita Kumari and **J.N.Roy:** Low power 7T SRAM cell Scheme- "Saving Write Zero Power": Conference and Exhibition on IP-SOC 2006: IP based SOC Design, Held at Grenoble- France, Dec.2006
53. **J.N.Roy:** Silicon On Insulator (SOI) Technology- An Overview: Proc. Of IMS Coference-2007, Held at Punjab Engineering College – Chandigarh in Aug.2007.
54. B.Umapathi, Sudipto Das Gupta, Vinita Mishra, Priya Hira and J.N.Roy: Design And Development of 1K × 1K Frame Transfer Imager: Proc. Of "Satellite Technology Day 2007"
55. Munish Mallik and **J.N.Roy:** Design of Low Voltage Differential Signaling (LVDS) Transmitter for Operation at 100 Mbps: Proc. Of IMS Coference-2007, Held at Punjab Engineering College – Chandigarh in Aug.2007.
56. Deep Sehgal and **J.N.Roy:**The design and Development of a High Performance Read-Out Integrated Circuit for Infrared Focal Plane Array: Proc. Of IMS

Coference-2007, Held at Punjab Engineering College (PEC) – Chandigarh in Aug.2007.

57. **J.N.Roy** Charge Coupled Device (CCD) Imagers: "Annals of INAE-2007"; an INAE Journal

58. **J.N.Roy** Nanotechnology and Nanocomputing: Recent Advances and Trends in Electrical Engineering, Held at NITTTR-Chandigarh in Feb.2008.
59. Manoj Wadhwa, Manish Hooda, Sanjay Verma and **J.N.Roy:** Micro Electro Mechanical Systems (MEMS)- a Technological Revolution: Recent Trends in Electronics and Communication: SUSCET-Mohali in April.2008.
60. Ayan Karmakar, Kamaljeet Singh, Manoj Wadhwa, Sanjay Verma and **J.N.Roy:** Characterization of Conductor backed finite ground co-planar waveguide: Recent Trends in Electronics and Communication: SUSCET_Mohali in April 2008.
60. Ashutosh Yadav, Rahul K. Tripathi, Rajesh K. Srivastava, Praveen Rana, H.S.Jatana and **J.N.Roy:** A 12-bit 1 Msample/s Pipelined Analog-to-Digital Converter: Proc. Of "Satellite Technology Day 2008"
61. Amit Chaudhry and **J.N.Roy:** Impact of Energy Quantization and Poly Depletion Effect on CV Analysis and Threshold Voltage of a n-MOSFET: International Conference on Semiconductor Electronics, ICSE-08, held in Malaysia, Oct. 2008.
62. Amit Chaudhry and **J.N. Roy**: "Modeling of Gate Leakage Current in High-K Dielectrics": Proceedings of 32nd IEEE International Convention on Information and Communication Technology, Electronics and Microelectronics, MIPRO, 2009 at Croatia, May, 2009, pp 79-84.
63. Amit Chaudhry and **J.N.Roy:** Analytical Modeling of Quantum Mechanical Tunneling in MOSFET: Proceeding of IEEE- Regional Symposium on Microelectronics (RSM), Malaysia, August, 2009, pp 22-27.
64. Amit Chaudhry and **J.N. Roy**: Quantum Mechanical Effects in MOSFETS: Journal of World Academy of Science, Engineering and Technology (WASET),Vol 58, 2009, pp 1445-1452.
65. Amit Chaudhry and **J.N.Roy:** Analytical Modeling of Energy Quantization effects in MOSFET: Proceeding of International Conference Microelectronics and Computer Science, Chisinuau, Moldova, Oct. 2009, pp 107-110.
66. **J.N.Roy**, Govadhan Rao Gariki and Nagalakshmi V.: Reference Module Selection Criteria for Accurate Testing of Photovoltaic (PV) Panels: Solar Energy, Vol.84, pp. 32-36, Jan., 2010.
67. Amit Chaudhry and **J.N.Roy:** MOSFET Models, Quantum Mechanical Effects and Modeling Approach: A Review: Journal of Semiconductor Science and Technology (JSST), June 2010.
68. Amit Chaudhry and **J.N.Roy:** Impact of quantum inversion charge centroid on the various parameters of a nano-MOSFET: Accepted for publication in the WASET International Conference on Microelectronic Devices, Rome, Italy, April, 2010.

69. Amit Chaudhry and **J.N.Roy:** Analytical Modeling of Quantum Mechanical Tunneling in Germanium Nano-MOSFET: Journal of Electronic Science and Technology, Vol.8, No.1, March 2010

70. Amit Chaudhry and **J. N. Roy:** Analytical Modeling of depletion and Energy Quantization in Poly Silicon of a Nano-MOSFET: ISC2010 Conference, Budapest, June 2010.

71. Amit Chaudhry and **J.N.Roy**: Analytical Modeling of Source-to-drain Tunneling In Nanoscale Silicon MOSFET: Journal of Electronics Science and Technology, Vol. 8, No. 4, December, 2010

72. Amit Chaudhry and **J.N.Roy:** Inversion Layer Quantization in Arbitrarily Oriented Substrates: An Analytical Study: ELEKTRIKA, Vol.12, No.1, December, 2010

73. Amit Chaudhry and **J.N. Roy:** Quantum Mechanical Direct leakage currents in a sub 10nm MOSFET: A Rigorous modeling study: International Journal of Nanoelectronics and Materials, (Accepted), 2011.

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75**.** Amit Chaudhry **and J.N. Roy:** Gate oxide leakage in poly-depleted nanoscale-MOSFET: A Quantum Mechanical Study: International Journal of Nanoelectronics and Materials, (Accepted), 2011.

76**.** Amit Chaudhry**, J.N. Roy** and S. Sangwan: A SPICE Compatible Analytical Electron Mobility Model for Biaxial Strained-Si-MOSFETs: Chinese Journal of Semiconductors, (Accepted), 2011.

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81. Amit Chaudhry and **J.N. Roy:** Comparative Study of Energy Quantization Approaches in nanoscale MOSFETS: Journal of Electronic Science and Technology, Vol.9, No.1, 2011.

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Poly Silicon Gate: Chinese Journal of Semiconductors, Vol.31, No.11, pp. 400-1-400-4, Nov, 2010.

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84. Amit Chaudhry and **J.N. Roy:** Impact of depletion and doping variation in poly gate and energy quantization in the substrate on gate leakage current in a nano-MOSFET: Proceedings of Prime Asia Conference on Post graduate Research in Microelectronics and Electronics, Shangai, China, Sept, 2010.
85. Amit Chaudhry and **J.N. Roy:** Gate capacitance modeling in (100), (110) and (111) oriented nanoscale MOSFET substrates: Proceedings of International Conference on Electrical and Computer Engineering, Dhaka, Bangladesh, Dec, 2010.
86. KVSR Kishore, Nazini S.K., Ashsih K Singh and **J.N.Roy:** Degradation Mechanism of Crystalline Solar Module from Damp Heat (DH) Test-to-Failure: 38th IEEE Photovoltaic Specialist Conference, June 3-8, 2012, Austin, Texas, USA.
87. **J N Roy:** Modeling of Insulation Characteristics of Solar Photovoltaic (SPV) Modules: Solar Energy, Vol. 120, pp 1-8, 2015.
88. Brajesh Kumar, **J N Roy** and Manab Das: Solar Energy Harvesting using Increase Heat Transfer Co-efficient and Absorption Rates, International Conference on Material Science & Technology, New Delhi, 2016, VBRI Press, DOI: 10-5185/icmtech.2016.
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PATENT APPLICATIONS:

1, Realization of Isolated Zener Diode in CMOS Process for Surge Protection and Voltage Regulation: **Patent No.: 232362, Application No.:374/DEL/1997, File No.:37/2008**
2. Novel Technique for Realization of Poly Silicon Fuses. **Patent No.:232406, Application No.:679/DEL/1997, File No.:21/2008**
3. A Vertical MOS Structure: **Patent No.: 232383, Application No.: 2625/DEL/1997, File No.:31/2008**
4. Embedded RFID Solution for Solar Panel: **US Patent No: 12/726,496, Publication No.: US2010/0236598 A1, Publication Date: Sept 23, 2010**