Name and Designation: Soumyajit Dey, Assistant Professor

Organization: Department of Computer Science and Engineering
Indian Institute of Technology Kharagpur
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Educational Qualification
Ph. D. Computer Science, Indian Institute of Technology Kharagpur, 2011;
M. S. Computer Science, Indian Institute of Technology Kharagpur, 2006;
B. E. Electronic and Telecommunication Engineering, Jadavpur University, Calcutta, India, June 2004.

Professional Experience (last 5)
2013 mid - now Assistant Professor, Computer Science and Engineering Dept, IIT Kharagpur, India
2012 Feb - 2013 mid Assistant Professor, Computer Science and Engineering Dept, IIT Patna, India
2011 mid – 2012 Jan Research Associate, School of Computing, National University Singapore

Specialization and Expertise: Formal Methods, Embedded Systems Design and Validation

Awards and Distinctions
- First Prize in the Design Contest held at the 19th International Conference on VLSI Design,2006.
- Winner of DST-Intel Technology Business Plan Contest 2006-07. Secured the first place at the national level and competed in the main event held at UC Berkeley, Haas School of Business.

Top ten publications in last ten years

1. Saurav Kumar Ghosh, Soumyajit Dey, Dip Goswami, Daniel Müller-Gritschneder and Samarjit Chakraborty, "Design and Validation of Fault-tolerant Embedded Controllers", DATE 2018
2. Sumana Ghosh, Soumyajit Dey and Pallab Dasgupta, "Co-synthesis of Loop Execution Patterns for Multi-Hop Control Networks", *IEEE Embedded Systems Letters*, November, 2017
3. Sumana Ghosh, Souradeep Dutta, Soumyajit Dey and Pallab Dasgupta, "A Structured Methodology for Pattern based Adaptive Scheduling in Embedded Control", ACM Transactions on Embedded Computing Systems (TECS), Volume 16, Issue 5s, September 2017, Article No. 189, Special Issue on EMSOFT 2017
4. Saurav Kumar Ghosh and Soumyajit Dey, "SERD: A Simulation Framework for Estimation of System Level Reliability Degradation", DATE 2017
5. Anirban Ghose, Lokesh Dokara, Soumyajit Dey, Pabitra Mitra, "A Framework for OpenCL Task Scheduling on Heterogeneous Multicore ", *Parallel Processing Letters* Vol. 27, No. 3-4 (2017)
6. Saurav Kumar Ghosh, Vishnuvardhan P, Satya Gautam Vadlamudi, Aritra Hazra, Soumyajit Dey, P. P. Chakrabarti, "RELSPEC: A Framework for Reliability Aware Design of Component based Embedded Systems", *Design Automation for Embedded Systems (Springer)*, Volume 21, Issue 1, pp 37–87, March 2017
7. Rajorshee Raha, Souradeep Dutta, Soumyajit Dey, Pallab Dasgupta, "Multi-rate Sampling for Power-Performance Trade-off in Embedded Control", *IEEE Embedded Systems Letters* , vol 8(4), pp 77-80 , 2016

8. Soumyajit Dey, Dipankar Sarkar, Anupam Basu "A Kleene Algebra of Tagged System Actors for Reasoning about Heterogeneous Embedded Systems", *IEEE Transaction Computers* , *vol 62(10), pp 1917-1931, 2013.*
9. Soumyajit Dey, Dipankar Sarkar, Anupam Basu "A Kleene Algebra of Tagged System Actors" - *IEEE Embedded Systems Letters*, *vol 3(1), pp 28-31, 2011*
10. Soumyajit Dey, Dipankar Sarkar, Anupam Basu "A Tag Machine based Performance Evaluation Method for Job-Shop Schedules", *IEEE Transaction CAD*, *vol 29(7), pp 1028-1041, 2010.*

Summary of research output (papers, patents, technology development): Published 11 articles in International Journals and 25 articles in International Conferences till date.

Five major sponsored R&D projects completed/handled

- Architecture and Algorithmic Optimizations for Speech based Communication Interfaces on Mobile Devices. (Sponsor: Intel Semiconductor (US) Limited, Valuation : 57 Lakhs INR, Role : PI) : 2013 – Ongoing,
- Synthesizing Test Programs as Directed Test Families for Incremental CPU Validation (Sponsor: Intel Semiconductor (US) Limited, Valuation : 24 Lakhs INR, Role : PI) : 2014 – Ongoing
- Intel Embedded Innovation Lablet (Sponsor: Intel Semiconductor (US) Limited, Valuation : 12 Lakhs INR, Role : PI) : 2013 - Ongoing
- An OpenCL Runtime System for Scheduling Data Parallel Workloads on Heterogeneous Clusters (DST Early Career Grant, Valuation: 50 Lakhs INR, Role : PI) : 2017 - 2020
- RTOS Validation and Development Support. (Sponsor: Hindusthan Aeronautics Limited, Valuation : 50 Lakhs, Role : Co-PI) : 2015 – Ongoing

Any other relevant information

Reviewer: IEEE TCAD, TC, TPDS, TCPS, ACM TOSEM ; Elsevier Theoretical Computer Science
PC Member: VLSI 2016, VDAT 2014, 2016

Dated 16th April 2018