

CURRICULUM VITAE

Dr. Pradip Mandal

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Date of birth: November 1, 1967.

Educational Qualifications:

Degree	Institution	Year	Department
Ph.D.*	I.I.Sc. Bangalore	1999	Electrical Comm. Engg.
M.E	I.I.Sc, Bangalore	1991	Electrical Comm. Engg
B.E	B.E. College, Cal Univ.	1989	Electronics & Tele-Comm

***Topic of the Ph.D. Thesis: Synthesis and Biasing of CMOS Op-Amps**

Professional Experience:

Academic:

- *Associate Professor* at the Dept. of Electronics and Electrical Communication Engineering, Indian Institute of Technology Kharagpur since 27th May 2011
- *Assistant Professor* at the Dept. of Electronics and Electrical Communication Engineering, Indian Institute of Technology Kharagpur From 24th May 2004 to 26th May 2011
- Teaching/taught *Analog Electronic Circuits* (UG), Introduction to Electronics (UG), *Analog VLSI Circuits* (PG), Semiconductor Device Modeling (PG) and VLSI Circuits and Systems (PG). Teaching feedback above four
- *Faculty Consultant* for different private organizations working in the area of analog IC design
- *Principle Investigator* of three research projects sponsored by Indian Govt organizations.
- Supervise Doctoral Thesis and Master level thesis (Successfully guided 5 Ph.D and 47 M.Tech/M.S thesis)
- Was Leading IC design activity in the Institution (through National Semiconductor foundry)
- Took initiative to get MoU signed with SCL Laboratory, enhancing collaboration opportunity to get our design implemented.
- Organized a Short-term course on “*CMOS Analog Design*” for Scientists of ISRO
- Delivered an Invited talk on “*An Overview of Input/Output Buffers*” in a National Conference
- Conducted on-site and on-line classes on “*Analog circuits*” through Talk to 10K teacher program at IIT Kharagpur
- Nine prototype Test Chips have been designed, got fabricated and tested for silicon validation of innovative circuits
- Overall citation of our 82 publications is 640 and the H-factor is 12.

Project Execution at IIT Kharagpur:

Sponsored (total cost Rs 90 L (approx)):

- Design Automation of Analog VLSI (AAV) Sponsored by DIT, Govt. of India.
- CMOS op-amp Design Automation in sub-micron technology (AST) Sponsored by: ISIRD, SRIC, IITKgp
- Design and Implementation of a 250 MSPS, 8 Bit ADC in Sub-Micron Technology for Space Application (BTA) Sponsored by ISRO, Govt. of India

Consultancy (total cost Rs 36 L (approx)):

- Power Supervisor and Voltage Regulator (PSVR) Sponsored by: Alliance Semiconductor (India) Pvt.Ltd.
- Equalizer for LiteLink (ELLP) Sponsored by: National Semiconductor Corporation, USA
- Design of Power Sequencer low voltage buck and PWM Controller (PWMC), Sponsored by: Alliance Semiconductor (India) Pvt. Ltd.
- I/O Buffer Design Review (IOBD), Sponsored by: Infineon Technology Pvt. Ltd.
- Design Methodology for robust analogue building blocks (DMRA), Sponsored by Sankalp Semiconductor Pvt. Ltd.
- Design of Switch Capacitor based Embedded DC-DC Buck Converter (DSBB) Sponsored by Maxim India Integrated Circuit.
- Design Methodology for analogue VLSI circuits (DAVC), Sponsored by Sankalp Semiconductor Pvt. Ltd.

Project Execution at Industries (prior to joining IIT Kharagpur):

- *More than 7 years hands-on experience with different responsibility, ranging from designer to design manager, in three different organizations*
- *As Design Manager with **Alliance Semiconductor (India) Pvt. Ltd.** From July 2002 to May 2004*

List of executed projects:

1. *Voltage Regulators* (in 0.13u and 0.18u process) for SRAM memory chip and mixed-signal chip
2. *Different high performance Input/Output buffers:* HSTL Tx & Rx (in 0.13u process), SSTL Tx & Rx (in 0.25u process) and LVDS Tx (in 0.35u process)
3. *Registered Buffers products* (in 0.25u process): for DDR DIMM application compliance to JEDEC standard
4. *Five Power Supervisor products* (in 0.5u process): for micro-controller, micro-processor application. Features include power on-, brownout-, manual-reset, Watchdog, Power fail, Battery backup switch, dual supply etc.
5. *Tuning/porting:* PLL - 50MHz – 200MHz (in 0.35u process), DLL -20MHz – 70MHz (in 0.35u process); ADC – 50MHz-10bit-pipeline (in 0.18u process)

- *As Design Architect with Philips Semiconductor division, **Philips Software Centre Pvt. Ltd., Bangalore,** From November 1998 to June 2002*

List of executed projects:

1. *LVC MOS Tx and Rx I/O* (in 0.35u, 0.25u and 0.18u process)
2. *I2C Tx and Rx I/O* (in 0.35u process)
3. *PECL Tx I/O* (in 0.35u process)
4. *SSTL Tx and Rx I/O* (in 0.35u process)
5. *USB 1.1 and USB 2.0 Tx and Rx I/O* (0.35u and 0.18u process)

- *As, Senior Software Engineer at **Motorola India Electronics Pvt. Ltd., Bangalore,** From February 1997 to October 1998*

List of executed projects:

1. *Focus:* An EDA tool for CMOS circuit sizing
2. *Nirvana:* An EDA tool for finger design of SAW filter

Areas of Research Interest:

- ❖ Design of Interface circuits for **High Speed Interconnect link** (both, off-chip and on-chip)
- ❖ Design of On-chip / on-package **Embedded Power Management module** for medium and low power applications
- ❖ Design of **Signal acquisition Front-end system** (containing Instrumentation amplifier, PGA and ADC)
- ❖ Parametric **Design Automation of CMOS analog circuits/systems** in sub-micron technology

Awards:

- Prof Arun Kumar Chaudury Best Paper Award at *the IEEE 21st International Conference on VLSI Design*, India, 2008
- Received *three* individual awards for submitting three circuit design Intellectual properties (IP) for patent application in Philips Software Centre Pvt. Ltd.
- Received a Team awards for best project in Philips Software Centre Pvt. Ltd.
- Received a Team awards for best project in Motorola India Electronics Pvt. Ltd

List of Patent granted/filed:

❖ Patent granted

1. **P. Mandal**, “ A Voltage limiting Semiconductor pass gate circuit”,
 - United State Patent 20050041343A1 Granted/Published on 24th Feb. 2005. (filed on 12th Dec 2002)
 - International Patent WO/2003/063198 Granted/Published on 31st July 2003 (filled on 12th Dec 2002)
2. A. Ali Khan, R. Pandey and **P. Mandal**, “Highest supply selecting circuit”, United States Patent No. US 7,298,181 B2 Granted/Published on Nov-2007 (filed 6th Dec. 2005)
3. P. Agarwal, M. Goel and **P. Mandal** “Circuit and Method to Convert a Single Ended Signal to Duplicated Signals”, United States Patent No US 7538,593,B2, Granted/Published on 26th May 2009 (filed 23rd Feb. 2007)

❖ Patent filled

1. **P. Mandal**, “Current mode Differential I/O Buffer unit for High Speed off-chip Interconnect” Filed for Indian Patent, Application No..557/KOL/2008..
2. Tamal Das and P. Mandal, ”A High Efficiency Charge Pump For Efficient DC-DC Step-Up Conversion for Thick Gate CMOS”, Filed for Indian Patent, Application No. 1765/KOL/200
3. P. K. Guha, R. Mukherjee, P. Mandal, 'An Advanced Thermal Accelerometer”, Filed for Indian Patent, Application No. 1075/KOL/2013, 20/03/2015
4. Joydeep Basu and P. Mandal, “An Integrated Signal acquisition cum Conditioning system application”, Filed for Indian Patent, Application No 1302/KOL/2015

❖ Patent provisionally filled

1. R. Mukherjee, P. K. Guha, P. Mandal, “Thermal Accelerometer with Active Temperature Sensor”, 201631001531, 15/01/2016.
2. R. Mukherjee, P. K. Guha, P. Mandal, Thermal Accelerometer with Improved Sensitivity”, 201631009720, 21/03/2016.

List of Publications (with citation number):

❖ Journal Papers

- 1) **P. Mandal** and V. Visvanathan, "Active Biasing of Multi Stage CMOS Op-Amps", *International Journal of Electronics, Taylor & Francis*, pg. 933-946, No.8, Vol. 86, Aug. 1999. (0)
- 2) **P. Mandal** and V. Visvanathan, "Self Biasing of High Performance Folded Cascode CMOS Op-Amp", *International Journal of Electronics, Taylor & Francis*, pp. 795- 808 No.9, Vol. 87, Aug. 2000. (5)
- 3) **P. Mandal** and V. Visvanathan, "CMOS Op-Amp Sizing Using a Geometric Programming Formulation", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, pg. 22-38, No. 1, Vol 20, Jan. 2001. (185)
- 4) Ashis Maiti, R. Raghavendra and **P. Mandal**, " Design of a low power voltage regulator for high dynamic range of load current", *International Journal of Electronics, Taylor & Francis*, pg 743-757, No. 8, Vol. 94, Aug. 2007 (8)
- 5) Tamal Das and **P. Mandal**, "Switched-Capacitor Based Buck Converter Design Using Current Limiter", *Journal of Low Power Electronics, American Scientific Publisher*, Vol. 5, NO 3, October 2009. (0)
- 6) Vijaya Sankara Rao P. and **P. Mandal** "Current-Mode Analog Interface for High-Speed Low-Current Differential Signaling" *International Journal of Electronics, Taylor & Francis*, Vol. 97(9), pg. 1007-1020, Sep. 2010 (0)
- 7) Vijaya Sankara Rao P. and **P. Mandal** "A new current-mode receiver for high-speed electrical/optical link ": *International Journal of Electronics and Communication, Elsevier*, Vol. 65, No.2, pg.107-116, Feb. 2011 (8)
- 8) Vijaya Sankara Rao P. and **P. Mandal**, "Active Terminated Transmitter and Receiver Circuits for High-Speed Low-Swing Duobinary Signaling", *International Journal of Circuit Theory and Applications, Wiley*, Vol. 40, No. 4, pp. 355–376, April 2012. (2)
- 9) Vijaya Sankara Rao P, Debashis Banerjee and **Pradip Mandal** "Active Terminated Current-Mode Pre-emphasis Transmitter for PCI Express Standard", *International Journal of Electronics and Communication, Elsevier*, Vol. 65, No. 7, pp. 650–July 2011, (1)
- 10) Kaushik Bhattacharyya and P. Mandal, "A Dynamically Reconfigurable NRTI Switched-Capacitor based Hybrid DC-DC Converter suitable for Embedded Applications", *Microelectronics Journal, Elsevier*, Vol. 42, No. 2, pp. 422–431, February 2011. (4)
- 11) Vijaya Sankara Rao P., Nachiket Desai and **P. Mandal**, "A Low Power 5Gb/s Current-Mode LVDS Output Driver with Active Termination", *Circuits, Systems and Signal Processing, Springer*, Vol. 31, No.1, pp 31-49, February 2012. (3)
- 12) Mrigank Sharad, Vijaya Sankara Rao P. and P. Mandal, "Half-Rate Duobinary Transmitter Architecture for Chip-to-Chip Interconnect Applications", *Analog Integrated Circuits and Signal Processing, Springer*, Vol. 68, No.3, pp 361-377, September 2011 (2)
- 13) Vijaya Sankara Rao P. and P. Mandal, "Current-Mode Full-Duplex (CMFD) Signaling for High Speed Chip-to-Chip Interconnect", *Microelectronics Journal, Elsevier*, Vol. 42, No. 7, pp. 957–965, July 2011, (4)
- 14) Biswajit Maiti and P. Mandal, "A High Performance Switched Capacitor Based DC-DC Buck Converter Suitable for Embedded Power Management Applications", *IEEE Trans. On VLSI*, Vol. 20, No.10, pp. 1880-1885, Oct. 2012. (22)
- 15) Kaushik Bhattacharyya, P. V. Ratna Kumar and Pradip Mandal, "Improvement of Power Efficiency and output voltage Ripple of Embedded DC-DC converters with Three Step Down ratios", *Journal of Circuits, Systems, and Computers, World Scientific*, Vol.21, No. 1, February 2012 (2)
- 16) Biswajit Maity, Soumya Gangula and Pradip Mandal, "Design and Implementation of an Area and Power Efficient Switched-Capacitor Based Embedded DC-DC Converter", *Journal of Low Power Electronics, American Scientific Publishers*, Vol. 8, No. 2, pp. 207-222(16), April 2012, (2)

- 17) Kaushik Bhattacharyya and Pradip Mandal, "Improvement of Performance of Dynamically Reconfigurable Switched Capacitor Based Non-Overlap Rotational Time Interleaved Embedded DC-DC Converter", *Journal of Low Power Electronics, American Scientific Publishers*, Vol. 8, No. 2, pp. 223-234(12), April 2012. (0)
- 18) Samiran Dam and Pradip Mandal, "Modeling and Design of CMOS Analog Circuits through Hierarchical Abstraction", *Integration, the VLSI Journal, Elsevier*, pp. 449-462, No. 4, Vol. 46, 2013. (3)
- 19) Debashis Mandal, Pradip Mandal, and Tarun Kanti Bhattacharyya, "A Spur Reducing Architecture of Frequency Synthesizer using Switched Capacitors", *IET Circuits, Devices Systems*, Vol. 8, No. 4, pp. 237–245, 2014, (0)
- 20) Tamal Das, Sankalan Prasad, Samiran Dam and Pradip Mandal, "A Pseudo Cross-Coupled Switch-Capacitor based DCDC Boost Converter for High Efficiency and High Power-Density", *IEEE Transactions on Power Electronics*, Vol. 29, No. 11, pp. 5961-5974, Nov, 2014 (7)
- 21) Sudip Kundu, and Pradip Mandal, "ISGP: Iterative Sequential Geometric Programming for Precise and Robust Analog Circuit Sizing", *Integration, the VLSI Journal, Elsevier*, pp. 510-531, Vol. 47, No. 4, 2014 (4)
- 22) Nijwm Wary and Pradip Mandal, "A low impedance receiver for power efficient current mode signaling across on-chip global interconnects", *International Journal of Electronics and Communications, Elsevier*, Volume 68, No.10, pp. 969–975, October 2014 (3)
- 23) Debashis Mandal, Pradip Mandal and Tarun Kanti Bhattacharyya, "Prediction of reference spur in frequency synthesizers", *IET Circuits, Devices Systems*, Vol. 9, No. 2, pp. 131–139, 2015, (2)
- 24) Nijwm Wary and Pradip Mandal, "High-speed energy-efficient bi-directional transceiver for on-chip global interconnects", *IET Circuits, Devices Systems*, Vol. 9, No. 5, pp. 319-327, 2015, (2)
- 25) R. Mukherjee, P.K. Guha, P. Mandal, 2016, 'Sensitivity improvement using optimized heater design for dual axis thermal accelerometers', *Microsystem Technologies*, Springer, vol. 22, No. 10, pp. 2475-2485. 2016, (DOI: 10.1007/s00542-015-2658-5) (2)
- 26) R. Mukherjee, P.K. Guha, P. Mandal, 2017, 'Sensitivity Improvement of A Dual Axis Thermal Accelerometer with Modified Cavity Structure', *Microsystem Technologies*, Springer, Vol. 23, No 12, pp. 5357-5363. November 2017 (DOI: 10.1007/s00542-017-3338-4) (1)
- 27) R. Mukherjee, J. Basu, P. Mandal, P. K.Guha, 2017, 'A review of micromachined thermal accelerometers.' *Journal of Micromechanics and Microengineering*, IOP Publishing vol. 27, no. 12: 123002, 2017, (DOI: 10.1088/1361-6439/aa964d) (0)
- 28) Nijwm Wary and Pradip Mandal, "Current-mode full-duplex transceiver for lossy on-chip global interconnects" *IEEE Journal of Solid-State Circuits*, Vol. 52, No.8, pp. 2026-2037, Aug. 2017. (0)
- 29) Nijwm Wary and Pradip Mandal, "Current-mode triline transceiver for coded differential signaling across on-chip global interconnects", *IEEE Trans. on VLSI*, Vol. 25, No.9, pp. 2575-2587, Sept. 2017. (0)
- 30) Sudip Kundu, and Pradip Mandal, "An efficient method of Pareto-optimal front generation for analog circuits", *Analog Integrated Circuits and Signal Processing, Springer*, pp. 289-316, Vol. 94, No. 2, 2018 (0)
- 31) Samiran Dam and Pradip Mandal, "An Integrated DC-DC Boost Converter having Low Output Ripple Suitable for Analog Applications," *IEEE Transactions on Power Electronics*, pp. 5108-5117, VOL. 33, NO. 6, JUNE 2018. (0)
- 32) Sabir Ali Mondal, Pradip Mandal and Hafizur Rahaman "Fast locking, startup-circuit free, low area, 32-phase analog DLL", *Integration, the VLSI Journal, Elsevier*, (Accepted)

❖ **International conference/ Symposium Papers**

- 1) **P. Mandal** and V. Visvanathan, "Macromodeling of the A.C. Characteristic of CMOS Op-Amps", *Proc. of IEEE International Conference on Computer Aided Design (ICCAD), Santa Clara, Nov. 1993.* (12)
- 2) **P. Mandal** and V. Visvanathan, "Design of High Performance two Stage CMOS Cascode Op-Amps with Stable Biasing", *Proc. of VLSI Design'96, IEEE Int. Conf. on VLSI Design, Bangalore, Jan. 1996* (3)
- 3) **P. Mandal** and V. Visvanathan, "A Self-Biased High Performance Folded Cascode CMOS Op-Amps", *Proc. of VLSI Design'97, IEEE Int. Conf. on VLSI Design, Hyderabad, Jan. 1997* (50)
- 4) **P. Mandal** and V. Visvanathan, "A New Approach for CMOS Op-Amp Synthesis", *Proc. of VLSI Design'99, IEEE Int. Conf. on VLSI Design, Goa, Jan. 1999* (9)
- 5) **P. Mandal**, "A narrow pulse suppressing filter for input buffer", *Proc. of VLSI Design'04, IEEE Int. Conf. on VLSI Design, Mumbai, Jan. 2004.* (2)
- 6) S.S. Prasad and **P. Mandal**, "A CMOS Beta Multiplier voltage reference with improved temperature performance and silicon tunability ", *Proc. of VLSI Design'04, IEEE Int. Conf. on VLSI Design, Mumbai, Jan. 2004.* (19)
- 7) Gunjan Mandal and **P. Mandal**, "Low Power LVDS transmitter with low common mode variation for 1 Gb/s-per pin operation", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS) Canada, May 2004* (25)
- 8) Ashis Maiti, R. Raghavendra and **P. Mandal**, "On-Chip Voltage Regulator with Improved Transient Response", *Proc. of VLSI Design'05, IEEE Int. Conf. on VLSI Design, Kolkata, Jan. 2005* (10)
- 9) Gunjan Mandal and **P. Mandal**, "Low Power LVDS Receiver for 1.3Gbps Physical Layer (Phy) Interface", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), Kobe, May 2005* (27)
- 10) Debashis Mandal and **P. Mandal**, "High Voltage tolerant Output Buffer design for Mixed Voltage Interface", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), Kobe, May 2005* (3)
- 11) S.S. Prasad and **P. Mandal**, "A Single circuit solution for Voltage Sensors", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), Kobe, May 2005* (0)
- 12) Kshitij Yadav and **P. Mandal**, "A VHF OTA-C topology having low phase error with Gm tuning", *ICCCAS, China, June 2006* (0)
- 13) **P. Mandal**, P.A.A. Khan and R. Pandey, "Max-Supply Selector using a Supply Voltage Comparator", *Mixed design of integrated circuits and Systems, Poland, June 2006* (1)
- 14) Kshitij Yadav and **P. Mandal**, "Design and Analysis of a VHF OTA-C Cell for Optimum Phase Response", *Proc. of IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Singapore, Dec. 2006* (0)
- 15) **P.Mandal** and Kaushik Bhattacharya, " A Low Voltage, Low Ripple on Chip Hybrid DC-DC Converter", *International Symposium on Integrated Circuits 2007, Singapore, Sept. 2007.* (5)
- 16) Rejeesh A.V. and **P. Mandal**, " A Fractional Frequency Synthesizer using Frequency Locked Loop", *IEEE International Conference on Electronics, Circuit and Systems (ICECS), Marrakech, Dec 11-14, 2007.* (2)

- 17) Kaushik Bhattacharyya **and P.Mandal**, "A Low Voltage, Low Ripple on Chip Dual Switch Capacitor Based Hybrid DC-DC Converter", *Proc. of VLSI Design'08, IEEE Int. Conf. on VLSI Design*, Hyderabad, Jan. 2008. (39)
- 18) Saurav Bandyopadhyay, **P.Mandal**, Stephen E. Ralph and Kenneth Pedrotti, "Integrated TIA-Equalizer for High Speed Optical Link", *Proc. of VLSI Design'08, IEEE Int. Conf. on VLSI Design*, Hyderabad, Jan. 2008. (13)
- 19) Samiran DasGupta and **P. Mandal**, "CMOS LDO Regulator Design using Geometric Programming", *IEEE Proc. of VLSI Design and Test Symposium*, Bangalore, July 2008. (0)
- 20) Samiran DasGupta and **P. Mandal**, "An Automated Design Approach for CMOS LDO Regulator", *IEEE Proc. of Asia and South Pacific Design Automation Conference*, Yokohama, Japan, Jan, 2009. (16)
- 21) Tamal Das and **P. Mandal**, "Switched-Capacitor Based Buck Converter Design Using Current Limiter for Better Efficiency and Output Ripple", *Proc. of VLSI Design'09, IEEE Int. Conf. on VLSI Design*, pg. 181-186, Delhi, Jan. 2009. (11)
- 22) Vijaya Sankara Rao P, **P. Mandal** and Sunil Sachdev "High Speed Low-Current Duobinary Signaling Over Active Terminated Chip-to-Chip Interconnect " *IEEE Computer Society Annual Symposium on VLSI*, Tampa, Florida, USA, May 13-15, 2009 (6)
- 23) **P. Mandal**, Sailesh Pati and Vijaya Sankara Rao P, "Active Terminated Differential Current-Mode Receiver for High-Speed Data Communication", *IEEE NEWCAS-TAISA'09*, Toulouse, France, June28-July 01, 2009 (2)
- 24) Vijaya Sankara Rao P, **P. Mandal** "Self-Termination Scheme for High-Speed Chip-to-Chip Data Communication" *IEEE International Symposium on Signals, Circuits and Systems*, Lasi, Romania, July 9-10, 2009. (0)
- 25) Vijaya Sankara Rao, Mrigank Sharad and **P. Mandal**, "High-Speed Transmitter for Fully Differential Current-Mode Polyquaternary Signaling Scheme", *IEEE International Midwest Symposium on Circuits and Systems(MWSCAS 2009)*, Cancun, Mexico, August 2-5, 2009 (2)
- 26) Kaushik Bhattacharyya, P. V. Ratnakumar and **P. Mandal**, "Embedded Hybrid DC-DC Converter with Improved Power Efficiency ", *52nd IEEE International Midwest Symposium on Circuits and Systems, 2009 (MWSCAS 2009)*, Cancun, Mexico, 2009 (7)
- 27) P.V. Ratnakumar, Kaushik Bhattacharyya, Tamal Das and **P. Mandal**, "Improvement of Power Efficiency in Switched Capacitor DC-DC Converter by Shoot-through Current Elimination", *ACM International Symposium on Low Power Electronics and Design (ISLPED)*, San Francisco, CA, USA 2009 (13)
- 28) Tamal Das and **P. Mandal**, "On-Chip Inductor-less DC-DC Boost Converter with Non-Overlapped Rotational Interleaving Scheme", *Proc. of VLSI Design'10, IEEE Int. Conf. on VLSI Design*, Bangalore, 2010 (1)
- 29) Samiran DasGupta and **P. Mandal**, "An Improvised MOS Transistor Model Suitable for Geometric Program Based Analog Circuit Sizing in Sub-micron Technology", *Proc. of VLSI Design'10, IEEE Int. Conf. on VLSI Design*, Bangalore, 2010 (16)
- 30) Vijaya Sankara Rao P, **P. Mandal**, "Current-Mode Echo Cancellation for Full-Duplex Chip-to-Chip Data Communication", *IEEE Asia Pacific Conference on Circuits and Systems*, Kuala Lumpur, Malaysia, 6-9 Dec. 2010. (0)
- 31) Vijaya Sankara Rao P, **P. Mandal** "A New Power Efficient Current-Mode 4-PAM Transmitter Interface for Off-Chip Interconnect", *IEEE Asia Pacific Conference on Circuits and Systems*, Kuala Lumpur, Malaysia, 6-9 Dec. 2010. (3)
- 32) Biswajit Maiti and **P. Mandal**, "A Switched-Capacitor Based Embedded DC-DC Buck Converter for High Power Efficiency and High Power Density", *Proc. of IEEE, TENCON 2010*, Fukuoka, Japan, Nov. 2010. (8)

- 33) Biswajit Maiti, Gaurav Bhagat and **P. Mandal**, "Dual Loop Push-Pull Feedback Linear Regulator for Embedded DC-DC Converter", *Proc. of IEEE, PEDES-2010*, New Delhi, India, Dec 2010 (2)
- 34) Biswajit Maiti, Gaurav Bhagat and **P. Mandal**, "Fast Transient Frequency Control Voltage Regulator Using Push-Pull Dynamic Leaker Circuit," *Proc. Of IEEE, India International Conference on Power Electronics*, New Delhi, India, Jan. 2011 (5)
- 35) Mrigank Sharad, Vijaya Sankara Rao P. and **P. Mandal**, "A New Double Data Rate Dual-Mode Duobinary Transmitter Architecture", *Proc. of VLSI Design'11, IEEE Int. Conf. on VLSI Design*, Chennai, India, January 2011. (2)
- 36) Sabyasachi Dewati and P. Mandal, "An Automated Design Methodology for Yield Aware Analog Circuit Synthesis in Submicron Technology", *International Symposium on Quality Electronic Design ISQED*, Santa Clara, USA, March 2011 (16)
- 37) Suprio Maji, Samiran Dam and P. Mandal, "Automatic Generation of Saturation Constraints and Performance Expressions for Geometric Programming Based Analog Circuit Sizing", *International Symposium on Quality Electronic Design ISQED*, Santa Clara, USA, March 2011 (12)
- 38) Suprio Maji and **P. Mandal**, "A Geometric Programming Aided Knowledge based Approach for Analog Circuit Synthesis and Sizing", *GLSVLSI, Lausanne*, Switzerland, May 2011 (6)
- 39) Supriyo Maji and Pradip Mandal, "An Efficient Methodology of Topology Selection and Sizing in Geometric Programming-Based Design Environment", *Design Automation Conference*, San Diego, CA, USA, June 5-9, 2011 (0)
- 40) Samiran Dam and Pradip Mandal, "Iterative Performance Model Up-gradation in Geometric Programming based Analog Circuit Sizing for Improved Design Accuracy", *25th International Conference on VLSI Design*, Hyderabad, India, January, 2012 (4)
- 41) Supriyo Maji and Pradip Mandal, "A Fast Equation Free Iterative Approach to Analog Circuit Sizing", *25th International Conference on VLSI Design*, Hyderabad, India, January, 2012 (6)
- 42) Pradip Mandal, Prajit Nandy and Mrinal Das, "Idea to Silicon: Challenges in Analog/Mixed Signal", *16th International Symposium on VLSI Design and Test*, Shibpur, India, July 1-4, 2012 (0)
- 43) Supriyo Maji, Pradip Mandal, "Efficient approaches to overcome non-convexity issues in analog design automation", *International Symposium on Quality Electronic Design*, USA, 2012 (0)
- 44) Biswajit Maity and Pradip Mandal, "Design of Push-Pull Dynamic Leaker Circuit for a Low Power Embedded Voltage Regulator", *16th International Symposium on VLSI Design and Test*, India, July 1-4, 2012 (0)
- 45) Debashis Mandal, Pradip Mandal, and Tarun Kanti Bhattacharyya, "Spur Suppression in Frequency Synthesizer using Switched Capacitor Array", *International SoC Design Conference (ISOCC)*, Jeju Island, Korea (South), 4-7 Nov, 2012 (5)
- 46) Avishek Biswas, Monodeep Kar and Pradip Mandal, "Techniques for Reducing Parasitic Loss in Switched-Capacitor based DC-DC Converter", *28th IEEE Applied Power Electronics Conference & Exposition*, Long Beach, California, USA, 17-21 March, 2013. (3)
- 47) Sudip. Kundu and Pradip Mandal, "A Generic and Efficient Modeling of Phase Margin of High Performance CMOS OpAmps", *IEEE Students' Technology Symposium*, Kharagpur, India, 2014. (0)
- 48) Soumya Bose and Pradip Mandal, "A Fully Differential Amplifier with CMOS Feedback Biasing for Sensing CMUT Signals", *IEEE Students' Technology Symposium*, Kharagpur, India, 2014. (0)
- 49) Nijwm Wary and Pradip Mandal, "Current-Mode Simultaneous Bidirectional Transceiver for On-Chip Global Interconnects", *IEEE 6th Asia Symposium on Quality Electronic Design*, 4-5th August, Kuala Lumpur, Malaysia, 2015. (2)
- 50) Samiran Dam, and Pradip Mandal, "A Stacked VCO Architecture for Generating Multi-Level Synchronous Control Signals," in *Proceedings of the 29th IEEE International Conference on VLSI*

Design and 15th International Conference on Embedded Systems (VLSID), January, 2016, pp. 151-155. (0)

51) Sudip Kundu and Pradip Mandal, "Design Automation of Analog Module using Hierarchical Decomposition", *IEEE Students' Technology Symposium*, Kharagpur, India, 2016. (0)

52) Joydeep Basu and Pradip Mandal, "Effect of switched-capacitor CMFB on the gain of fully differential op-amp for design of integrators," in *Proc. of 2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, pp. 1–5, May. 2018.

53) Antroy Roy Chowdhury, Nijwm Wary and Pradip Mandal, "Energy Efficient Bidirectional Equalized Transceiver with PVT Insensitive Active Termination," in *Proceedings of the 32th IEEE International Conference on VLSI Design and 18th International Conference on Embedded Systems (VLSID)*, January, 2019

Submitted manuscripts:

In Journal:

Antroy Roy Chowdhury, Nijwm Wary and Pradip Mandal, "Energy Efficient Bidirectional Equalized Transceiver with PVT Insensitive Active Termination," under revision in *the Special Issue: Energy-efficient Computing for Embedded and IoT Devices for the IET Computers & Digital Techniques*.

Joydeep Basu and Pradip Mandal, "Delta-Sigma Modulator based Compact Signal Acquisition Front-end System", submitted to *IEEE Transactions on Circuits and Systems I*

Nishant Mehrotra, Joydeep Basu and Pradip Mandal, "A Concurrent Design and Optimization Technique for Discrete-Time Dual-Quantization Delta-Sigma Modulators", submitted to *Microelectronics Journal, Elsevier*

In Conference:

Antroy Roy Chowdhury, Nijwm Wary and Pradip Mandal, "A Regulated-Cascode Based Current-Integrating TIA RX with 1-tap Speculative Adaptive DFE", submitted to *MWSCAS*, Dallas, TX, USA, Aug. 2019.