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EDUCATION

- **Ph.D.** in Computer Engineering, Department of Electrical Engineering and Computer Science, Case Western Reserve University, Cleveland, Ohio, USA.
Duration: Aug. 2006 - May 2010
Advisor: Prof. Swarup Bhunia
Dissertation: **Hardware Security through Design Obfuscation**
CGPA: 4.00/4.00
- **B.E. (Honors)** in Electronics and Telecommunication Engineering, Jadavpur University, Kolkata, India.
Duration: 2001 - 2005
CGPA: 86.84%

PROFESSIONAL EXPERIENCE

- **Associate Dean**, *Faculty of Engineering and Architecture*, Indian Institute of Technology Kharagpur, Kharagpur, West Bengal, India (Aug. 2023 – Aug. 2025)
- **Professor**, *Dept. of Computer Science and Engineering*, Indian Institute of Technology Kharagpur, Kharagpur, West Bengal, India (Mar. 2023- present)
- **Offensive Security Researcher**, Intel Corporation, Bangalore, India [on leave from IIT Kharagpur], (Dec. 2021- Feb. 2023)
- **Associate Professor**, *Dept. of Computer Science and Engineering*, Indian Institute of Technology Kharagpur, Kharagpur, West Bengal, India (Feb. 2016 – Feb. 2023)

- **Assistant Professor**, *Dept. of Computer Science and Engineering*, Indian Institute of Technology Kharagpur, Kharagpur, West Bengal, India (Jun. 2010 – Feb. 2016)
- **Engineering Co-op**, *Advanced Micro Devices (AMD)*, Sunnyvale, CA, USA (Sep. 2007-Dec. 2007)
- **CAD Software Engineer**, *National Semiconductor*, Bangalore, India (Jul. 2005-Jul. 2006)
- **Engineering Co-op**, *National Semiconductor*, Bangalore, India (Jun. 2004-Aug. 2004)

RESEARCH AND PUBLICATIONS

- **Research Interests:**
 - Hardware Security
 - Electronic Design Automation
 - VLSI
 - Digital Image Forensics
- **Edited Volume**
 1. S. Roy, **R. S. Chakraborty** and A. Sarkar (eds.), “Statistics for Data and Predictive Analysis”, *Apple Academic Press*, in press.
 2. S. Roy, **R. S. Chakraborty**, J. Mathew, A. P. Mazumdar and S. Chakraborty (eds.) “Artificial Intelligence and Deep Learning for Computer Network: Management and Analysis”, *CRC Press* (ISBN: 9781032079592 print, 9781003212249 e-book), 2023.
 3. **R. S. Chakraborty**, J. Mathew and A. V. Vasilakos (eds.), “Security and Fault Tolerance in Internet of Things”, *Springer* (ISBN: 9783030028060 print, ISBN: 9783030028077 e-book), 2019.
 4. **R. S. Chakraborty**, P. Schwabe and J. Solworth (eds.), “Proceedings of the 5th International Conference on Security, Privacy and Applied Cryptography Engineering (SPACE) 2015”, *Lecture Notes in Computer Science* vol. 9354, *Springer*, 2015.
 5. **R. S. Chakraborty**, V. Matyas and P. Schaumont (eds.), “Proceedings of the 4th International Conference on Security, Privacy and Applied Cryptography Engineering (SPACE) 2014”, *Lecture Notes in Computer Science* vol. 8804, *Springer*, 2014.
- **Books**
 1. S. Roy, P. Santikellur and **R. S. Chakraborty**, “Machine Learning and Deep Learning Meet Computer Networks”, *Springer* (forthcoming).
 2. P. Santikellur and **R. S. Chakraborty**, “Deep Learning for Computational Problems in Hardware Security: Modeling Attacks on Strong Physically Unclonable Function Circuits”, *Springer* (ISBN: 9789811940163 print, 978-981-19-4017-0 e-book), 2023.
 3. A. Roy, R. Dixit, R. Naskar and **R. S. Chakraborty**, “Digital Image Forensics - Theory and Implementation”, *Springer* (ISBN: 9789811076435 print, 9789811076442 e-book), 2020.
 4. A. Palchadhuri and **R. S. Chakraborty**, “High Performance Integer Arithmetic Circuit Design on FPGA: Architecture, Implementation and Design Automation”, *Springer* (ISBN: 9788132225195 print, 9788132225201 e-book), 2016.
 5. D. Mukhopadhyay and **R. S. Chakraborty**, “Hardware Security: Design, Threats and Safeguards”, *CRC Press* (USA) (ISBN: 9781439895832), 2015.

6. R. Naskar and **R. S. Chakraborty**, “Reversible Digital Watermarking: Theory and Practices”, *Morgan Claypool* (USA), (ISBN: 9781627053150 print, ISBN: 9781627053167 e-book), 2014.

- **Book Chapters**

1. P. Santikellur, **R. S. Chakraborty** and S. Bhunia, "Hardware IP Protection Using Register Transfer Level Locking and Obfuscation of Control and Data Flow" in S. Katkooi and S. A. Islam (eds.), "Behavioral Synthesis for Hardware Security", *Springer*, 2022 (ISBN 978-3-030-78840-7 print, ISBN 978-3-030-78841-4 (eBook)).
2. S. R. Rajendran and **R. S. Chakraborty**, “Online Checkers to Detect Hardware Trojans in AES Hardware Accelerators”, in S. Saini, K. Lata and G. R. Sinha (eds.), “VLSI and Hardware Implementations Using Modern Machine Learning Methods”, *CRC Press*, 2022 (ISBN: 9781003201038).
3. **R. S. Chakraborty** and R. Mukherjee, “FPGA Security (invited chapter)”, in S. Sajodia, P. Samarati and M. Yung (eds.), “Encyclopedia of Cryptography, Security and Privacy”, *Springer*, 2019 (ISBN: 9783642277399).
4. P. Santikellur, **R. S. Chakraborty** and J. Mathew, “Hardware Security in the Context of Internet of Things: Challenges and Opportunities”, in U. Ghosh, D. B. Rawat, R. Datta and A. K. Pathan (eds.), “Internet of Things and Secure Smart Environments: Success and Pitfalls”, *CRC Press*, 2020 (ISBN: 9780367276706).
5. V. Govindan and **R. S. Chakraborty**, "Logic Testing for Hardware Trojan Detection", in S. Bhunia and M. Tehranipoor (eds.), "The Hardware Trojan War: Attacks, Myths, and Defenses", *Springer*, 2017 (ISBN: 9783319685106).
6. **R. S. Chakraborty** and S. Bhunia, “State Space Obfuscation and its Applications in Hardware Security”, in D. Forte, S. Bhunia and M. Tehranipoor (eds.), “Hardware Protection through Obfuscation”, *Springer*, 2017 (ISBN: 9783319490199).
7. R. Naskar, P. Malaviya and **R. S. Chakraborty**, “Digital Forensics: State-of-the-Art and Open Problems”, in R. Pal (ed.), “Innovative Research in Attention Modeling for Computer Vision Applications”, *IGI Global*, 2015 (ISBN: 9781466687233 print, ISBN: 9781466687240 e-book).
8. A. Palchaudhuri and **R. S. Chakraborty**, “A Fabric Component based Approach to the Architecture and Design Automation of High Performance Integer Arithmetic Circuits on FPGA”, in M. Fakhfakh, E. Tlelo-Cuautle and P. Siarry (eds.), “Computational Intelligence in Analog and Mixed-Signal (AMS) and Radio-Frequency (RF) Circuit Design”, *Springer*, 2015 (ISBN: 9783319198712 print, ISBN: 9783319198729 e-book).
9. **R. S. Chakraborty**, S. Bhunia and Y. Zheng, “RTL IP Protection and Secure SoC Design: a Design Obfuscation based Approach”, in C. H. Chang and M. Potkonjak (eds.), “Secure System Design and Trustable Computing”, *Springer*, 2015 (ISBN: 9783319149707 print, ISBN: 9783319149714 e-book).
10. R. Naskar and **R. S. Chakraborty**, “Reversible Watermarking: Theory and Practice”, in B. Issac (ed.), “Case Studies in Secure Computing – Achievements and Trends”, *CRC Press*, 2014 (ISBN: 9781482207064 print, ISBN: 9781482207071 e-book).
11. R. Naskar, **R. S. Chakraborty**, D. K. Das and C. Chakraborty, “Digital Image Watermarking: Impact on Medical Imaging Applications in Telemedicine”, in Dr. R.

Srivastava (ed.), "Recent Advances in Computer Vision and Image Processing: Methodologies and Applications", *IGI Global*, 2013 (ISBN 9781466645585).

- **Journal Papers** (in reverse chronological order)

1. R. Mukherjee and **R. S. Chakraborty**, "Detecting Hardware Trojans in High-Level Synthesis-Generated RTL using Large Language Models", accepted in *ACM Transactions on Design Automation of Electronic Systems*.
2. A. Bhattacharyya, R. P. Behera, A. Dasgupta and **R. S. Chakraborty**, "Uncertainty-Aware Remaining Useful Life Estimation for Aluminium Electrolytic Capacitors Using Spectral Mixture Kernels and Hybrid Uncertainty Calibration", accepted in *IEEE Transactions on Reliability*.
3. Gisha C. G., A. S. Chakraborty, **R. S. Chakraborty**, B. A. Jose and J. Mathew, "Challenges in Modelling Analog PUFs: A Study of Hybrid and Diode Triode Current Mirror Inverter PUF under Machine Learning Attacks", accepted in *IET Computers and Digital Techniques*.
4. A. Dutta, S. Roy and R. S. Chakraborty, "RISK-4-Auto: Residually Interconnected and Superimposed Kolmogorov-Arnold Networks for Automotive Network Traffic Classification", *IEEE Transactions on Network and Service Management*, vol. 23, pp. 1076-1085, Oct. 2025.
5. D. Das, R. Naskar and **R. S. Chakraborty**, "Image Splicing Localization based on Hellinger Distance and Noise Estimation through Convolutional Neural Network and Vision Transformer", *Digital Signal Processing* (Elsevier), vol. 2026 (part B), Jan. 2026.
6. A. Bhattacharyya, A. Dutta, R. P. Behera, A. Dasgupta and **R. S. Chakraborty**, "POFINN: Integrating Physics of Failure and Neural Networks for Long-term Degradation Forecasting of Aluminium Electrolytic Capacitors", *IEEE Transactions on Reliability*, vol. 74, no. 4, pp. 5487-5501, Dec. 2025.
7. A. K. Das, A. Bose, P. Manohar; A. Dutta, R. Naskar and **R. S. Chakraborty**, "InDeepFake: A Novel Multimodal Multilingual Indian Deepfake Video Dataset", *Pattern Recognition Letters* (Elsevier), vol. 197, pp. 16-23, Nov. 2025.
8. S. Roy and **R. S. Chakraborty**, "Low-Cost Smart Irrigation Solution for Efficient Water Use and Requirement Prediction", *Computers and Electrical Engineering* (Elsevier), vol. 125, Jul. 2025.
9. A. Dutta, S. P. Nayak, R. Naskar and **R. S. Chakraborty**, "KOL-4-GEN: Stacked Kolmogorov-Arnold and Generative Adversarial Networks for Malware Binary Classification through Visual Analysis", *IEEE Embedded Systems Letters*, vol 17, no. 4, pp. 268-271, Aug. 2025.
10. S. Swaroopa, R. Mukherjee, A. Debnath and **R. S. Chakraborty**, "Evaluating Large Language Models for Automatic Register Transfer Logic Generation for Combinational Circuits via High-Level Synthesis", *Foundations and Trends in Electronic Design Automation* (special issue on "Harnessing the Potential of Deep-learning Algorithms and Generative AI for SoC and Chiplet Design and Verification"), vol. 14. no. 4, pp 315-337, May 2025.
11. S. Swaroopa, M. Manivannan, **R. S. Chakraborty** and I. Chakrabarti, "A Provably Secure Scheme to Prevent Master Key Recovery by Fault Attack on AES Hardware", *IEEE Embedded Systems Letters*, vol. 16, no. 4, pp. 521-524, Dec. 2024.
12. K. Pratihar, **R. S. Chakraborty** and D. Mukhopadhyay, "Latent RAGE: Randomness Assessment using Generative Entropy Models", accepted in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 43, no. 11, pp. 3503-3514, Nov. 2024 [part of *ACM/IEEE ESWEEK 2024*].
13. K. Pratihar, S. Chatterjee, **R. S. Chakraborty** and D. Mukhopadhyay, "Enhancing SRAM-Based PUF Reliability Through Machine Learning-Aided Calibration Techniques", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 43, no. 11, pp. 3491-3502, Nov. 2024. [part of *ACM/IEEE ESWEEK 2024*].

14. R. Mukherjee and **R. S. Chakraborty**, "HLS-IRT: Hardware Trojan Insertion through Modification of Intermediate Representation During High-Level Synthesis", *ACM Transactions on Design Automation of Electronics Systems*, vol. 29, no. 5, pp. 1-23, Sep. 2024.
15. S. Manivannan, **R. S. Chakraborty**, I. Chakrabarti and J. Rangasamy, "Practical and Efficient PUF-based Protocol for Authentication and Key Agreement in IoT", *IEEE Embedded Systems Letters*, vol. 16, no. 2, pp. 118-121, Jun. 2024.
16. M. Mahalat, S. Subba, A. Mondal, B. K. Sikdar, **R. S. Chakraborty** and B. Sen, "CAPUF: Design of a Configurable Circular Arbiter PUF with Enhanced Security and Hardware Efficiency", *Integration, the VLSI Journal* (Elsevier), vol. 95, pp. 102-113, Mar. 2024.
17. Gisha C. G., A. S. Chakraborty, **R. S. Chakraborty**, B. A. Jose and J. Mathew, "A Novel Physical Unclonable Function based on Hybrid Current Mirror", *Journal of Hardware and Systems Security* (Springer), vol. 7, pp. 125-137, Dec. 2023.
18. R. Mukherjee and **R. S. Chakraborty**, "Attacks on Recent DNN IP Protection Techniques and Their Mitigation", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 42, no. 11, pp. 3642-3650, Nov. 2023.
19. D. Das, R. Naskar and **R. S. Chakraborty**, "Image Splicing Detection with Principal Component Analysis Generated Low-dimensional Homogeneous Feature Set based on Local Binary Pattern and Support Vector Machine", *Multimedia Tools and Applications* (Springer), vol. 82, no. 17, pp. 25847-25864, Jul. 2023.
20. K. Pratihar, U. Chatterjee, M. Alam, D. Mukhopadhyay, and **R. S. Chakraborty**, "Birds of the Same Feather Flock Together: A Dual-Mode Circuit Candidate for Strong PUF-TRNG Functionalities", *IEEE Transactions on Computers*, vol. 72, no. 6, pp. 1636-1651, Jun. 2023.
21. D. Singh, P. Singh, R. Jena and **R. S. Chakraborty**, "An Image Forensic Technique Based on JPEG Ghosts", *Multimedia Tools and Applications* (Springer), vol. 82, no. 9, pp. 14153-14169, Apr. 2023.
22. P. Santikellur, M. Buddhanoy, S. Sakib, B. Ray and **R. S. Chakraborty**, "A Shared Page-Aware Machine Learning Assisted Method for Predicting and Improving Multi-Level Cell NAND Flash Memory Life Expectancy", *Microelectronics Reliability* (Elsevier), vol. 140, pp. 114867, Jan. 2023.
23. P. Santikellur and **R. S. Chakraborty**, "Correlation Integral based Intrinsic Dimension: a Deep Learning Assisted Empirical Metric to Estimate the Robustness of Physically Unclonable Functions to Modeling Attacks", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 4, pp. 3216-3227, Oct. 2022.
24. R. Mukherjee, S. R. Rajendran and **R. S. Chakraborty**, "A Comprehensive Survey of Physical and Logic Testing Techniques for Hardware Trojan Detection and Prevention", *Journal of Cryptographic Engineering* (Springer), vol. 12, no. 4, pp. 495-522, Nov. 2022. Note: This is an extended version of the paper published in ACM International Workshop on Attacks and Solutions in Hardware Security (ASHES), [post-conference workshop co-located with ACM CCS], Virtual Workshop, Nov. 2020.
25. R. Mukherjee and **R. S. Chakraborty**, "Novel Hardware Trojan Attack on Activation Parameters of FPGA-based DNN Accelerators", *IEEE Embedded Systems Letters*, vol. 14, no. 3, pp. 131-134, Sep. 2022.
26. M. H. Mahalat, S. Mandal, A. Mondal, B. Sen and **R. S. Chakraborty**, "Implementation, Characterization and Application of Path Changing Switch based Arbiter PUF on FPGA as a lightweight Security Primitive for IoT", *ACM Transactions on Design Automation of Electronic Systems*, vol. 27, no. 3, pp. 26:1-26:26, May 2022.
27. A. Saha, H. Banerjee, **R. S. Chakraborty** and D. Mukhopadhyay, "ORACALL: An Oracle-Based Attack on Cellular Automata Guided Logic Locking", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 12, pp. 2445-2454, Dec. 2021.

28. S. Chattopadhyay, P. Santikellur, **R. S. Chakraborty**, J. Mathew and M. Ottavi, "A Conditionally Chaotic Physically Unclonable Function Design Framework with High Reliability", *ACM Transactions on Design Automation of Electronic Systems*, vol. 26, no. 6, pp. 41:1-41:24, Nov. 2021.
29. P. Santikellur and **R. S. Chakraborty**, "A Computationally Efficient Tensor Regression Network based Modeling Attack on XOR Arbiter PUF and its Variants", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 6, pp. 1197-1106, Jun. 2021.
30. R. Mukherjee, V. Govindan, S. Koteswara, A. Das, K. K. Parhi and **R. S. Chakraborty**, "Probabilistic Hardware Trojan Attacks on Multiple Levels of Reconfigurable Network Infrastructure", *Journal of Hardware and Systems Security* (Springer), vol. 4, no. 4, pp. 343-360, Dec. 2020.
31. A. Chakraborty, V. Maurya, S. Prasad, S. Gupta, **R. S. Chakraborty** and H. Rahaman, "BDD-based Synthesis Technique for improved mapping of Boolean functions inside Memristive crossbar-slices", *IET Computers and Digital Techniques*, vol. 15, no. 4, pp. 112-124, Dec. 2020.
32. U. Chatterjee, D. Mukhopadhyay and **R. S. Chakraborty**, "3PAA: A Private PUF Protocol for Anonymous Authentication", *IEEE Transactions on Information Forensics and Security*, vol. 16, pp. 756-769, Sep. 2020.
33. A. Roy and **R. S. Chakraborty**, "Towards Optimal Prediction Error Expansion based Reversible Image Watermarking", *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 30, no. 8, pp. 2377-2390, Aug. 2020.
34. U. Chatterjee, S. Chatterjee, D. Mukhopadhyay and **R. S. Chakraborty**, "Machine-Learning Assisted PUF Calibration for Trustworthy Proof of Sensor Data in IoT", *ACM Transactions on Design Automation of Electronic Systems*, vol. 25, no. 4, pp. 32:1-32:21, Jun. 2020.
35. T. Hoque, **R. S. Chakraborty** and S. Bhunia, "Hardware Obfuscation and Logic Locking: a Tutorial Introduction", *IEEE Design & Test*, vol. 37, no. 3, pp. 59-77, Mar. 2020.
36. V. K. Rai, S. Tripathy, **R. S. Chakraborty** and J. Mathew, "HTRNG: High Throughput True Random Number Generator using Memristor", *IEEE VLSI Circuits & Systems Letter* (feature article), vol. 6, no. 1, pp. 1-12, Feb. 2020.
37. P. Ghosh, A. Bhattacharyay, D. Forte and **R. S. Chakraborty**, "Automated Defective Pin Detection for Recycled Microelectronics Identification", *Journal of Hardware and Systems Security* (Springer), vol. 3, no. 3, pp. 250-260, Sep. 2019.
38. D. B. Tariang, **R. S. Chakraborty** and R. Naskar, "A Robust Residual Dense Neural Network for Countering Anti-Forensic Attack on Median Filtered Images", *IEEE Signal Processing Letters*, vol. 26, no. 8, pp. 1132-1136, Aug. 2019.
39. P. Ghosh and **R. S. Chakraborty**, "Recycled and Remarketed Counterfeit Integrated Circuit Detection by Image Processing based Package Texture and Indent Analysis", *IEEE Transactions on Industrial Informatics*, vol. 15, no. 4, pp. 1966-1974, Apr. 2019.
40. V. Govindan, **R. S. Chakraborty**, P. Santikellur and A. K. Chaudhary, "A Hardware Trojan Attack on FPGA based Cryptographic Key Generation: Impact and Detection", *Journal of Hardware and Systems Security* (Springer), vol. 2, no. 3, pp. 225-239, Sep. 2018.
41. U. Chatterjee, V. Govindan, R. Sadhukhan, D. Mukhopadhyay, **R. S. Chakraborty**, D. Mahata and M. Prabhu, "Building PUF based Authentication and Key Exchange Protocol for IoT without Explicit CRPs in Verifier Database", *IEEE Transactions on Dependable and Secure Computing*, vol. 16, no. 3, May/June. 2019, pp. 424-437.
42. D. Basu Roy, M. Alam, S. Bhattacharya, V. Govindan, F. Regazzoni, **R. S. Chakraborty** and D. Mukhopadhyay, "Customized Instructions for Protection Against Memory Integrity Attacks", *IEEE Embedded Systems Letters*, vol. 10, no. 3, pp. 91-94, Sep. 2018.

43. D. P. Sahoo, D. Mukhopadhyay, **R. S. Chakraborty** and P. H. Nguyen, "A Multiplexer-Based Arbiter PUF Composition with Enhanced Reliability and Security", *IEEE Transactions on Computers*, vol. 67, no. 3, pp. 403-417, Mar. 2018.
44. Anju P. Johnson, S. Patranabis, **R. S. Chakraborty** and D. Mukhopadhyay, "Remote Dynamic Partial Reconfiguration: A Threat to Internet-of-Things and Embedded Security Applications", *Microprocessors and Microsystems* (Elsevier), vol. 52, no. C, pp. 131-144, Jul. 2017.
45. **R. S. Chakraborty**, Samuel Pagliarini, J. Mathew, Sree Ranjani R. and Nirmala Devi M., "A Flexible Online Checking Technique to Enhance Hardware Trojan Horse Detectability by Reliability Analysis", *IEEE Transaction on Emerging Topics in Computing*, vol. 5, no. 2, pp. 260-270, Jan. 2017.
46. U. Chatterjee, **R. S. Chakraborty** and D. Mukhopadhyay, "A PUF based Secure Communication Protocol for IoT", *ACM Transactions on Embedded Computing Systems*, vol. 16, no. 3, pp. 67:1-67:25, Jul. 2017.
47. **R. S. Chakraborty**, R. R. Jeldi, I. Saha and J. Mathew, "Binary Decision Diagram Assisted Modeling of FPGA-based Physically Unclonable Function by Genetic Programming", *IEEE Transaction on Computers*, vol. 66, no. 6, pp. 971-981, Jun. 2017.
48. P. H. Nguyen, D. P. Sahoo, **R. S. Chakraborty** and D. Mukhopadhyay, "Security Analysis of Arbiter PUF and its Lightweight Compositions under Predictability Tests", *ACM Transactions on Design Automation of Electronic Systems*, vol. 22, no. 2, pp. 20:1-20:28, Feb. 2017.
49. Anju P. Johnson, **R. S. Chakraborty** and D. Mukhopadhyay, "An Improved DCM-based Tunable True Random Number Generator for Xilinx FPGA", *IEEE Transactions on Circuits and Systems-II*, vol. 64, no. 4, pp. 452-456, April 2017.
50. Y. Yang, J. Mathew, **R. S. Chakraborty**, M. Ottavi and D. K. Pradhan, "Low Cost Memristor Associative Memory Design for Full and Partial Matching Applications", *IEEE Transactions on Nanotechnology*, vol. 15, no. 2, pp. 537-538, May 2016.
51. Anju P. Johnson, **R. S. Chakraborty** and D. Mukhopadhyay, "A PUF-enabled Secure Architecture for FPGA-based IoT Applications", *IEEE Transactions on Multi-scale Computing Systems* (special issue on *Wearables, Implants and Internet-of-Things*), vol. 1, no. 2, pp. 110-122, April-June 2015.
52. U. Chatterjee, **R. S. Chakraborty**, H. Kapoor and D. Mukhopadhyay, "Theory and Application of Delay Constraints in Arbiter PUF", *ACM Transactions on Embedded Computing Systems*, vol. 15, no. 1, Feb. 2016, pp. 10:1-10:20.
53. D. P. Sahoo, P. H. Nguyen, D. Mukhopadhyay and **R. S. Chakraborty**, "A Case of Lightweight PUF Constructions: Cryptanalysis and Machine Learning Attacks", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 8, Aug. 2015, pp. 1334 - 1343.
54. J. Mathew, **R. S. Chakraborty**, Y. Yang, D. P. Sahoo and D. Pradhan, "A Novel Memristor based Physically Unclonable Function", *Integration, the VLSI Journal* (Elsevier), vol. 51, Sep. 2015, pp. 37-45.
55. R. Naskar and **R. S. Chakraborty**, "A Technique to Evaluate Upper Bounds on Performance of Pixel-Prediction based Reversible Watermarking Algorithms", *Journal of Signal Processing Systems* (Springer), vol. 82, no. 3, Mar. 2016, pp. 373-389.
56. J. Mathew, **R. S. Chakraborty**, Y. Yang, D. P. Sahoo and D. Pradhan, "A Novel Memristor based Hardware Security Primitive", *ACM Transactions on Embedded Computing Systems*, vol. 14, no. 3, pp. 60:1-60:20, May 2015.
57. S. Narasimhan, D. Du, **R. S. Chakraborty**, S. Paul, F. Wolff, C. Papachristou, K. Roy and S. Bhunia, "Hardware Trojan Detection by Multiple-Parameter Side-Channel Analysis", *IEEE Transactions on Computers*, vol. 62, no. 11, Nov. 2013, pp. 2183-2195.

58. **R. S. Chakraborty**, I. Saha, A. Palchoudhuri and G. K. Naik, "Hardware Trojan Insertion by Direct Modification of FPGA Configuration Bitstream", *IEEE Design & Test of Computers*, vol. 30, no. 2, Apr. 2013, pp. 45-54 (**most popular article in IEEE Design & Test of Computers in the period April-July 2013**).
59. R. Naskar and **R. S. Chakraborty**, "A Generalized Tamper Localization Approach for Reversible Watermarking Algorithms", *ACM Transactions on Multimedia Computing Communications and Applications*, vol. 9, no. 3, Jun. 2013, pp. 19:1-19:22.
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61. S. Goren, O. Ozkurt, A. Yildiz, H. Fatih Ugurdag, **R. S. Chakraborty** and D. Mukhopadhyay, "Partial Bitstream Protection for Low-cost FPGAs with PUFs, Obfuscation & DPSR-LD", *Computers and Electrical Engineering (Elsevier)*, vol. 39, no. 2, Feb. 2013, pp. 386-397.
62. R. Naskar and **R. S. Chakraborty**, "Performance of Reversible Digital Image Watermarking under Error-prone Data Communication: a Simulation-based Study", *IET Image Processing*, vol. 6, no. 6, Aug. 2012, pp. 728-737.
63. R. Naskar and **R. S. Chakraborty**, "Reversible Watermarking Utilizing Weighted-median based Prediction", *IET Image Processing*, vol. 6, no. 5, Jul. 2012, pp. 507-520.
64. S. Narasimhan, S. Bhunia and **R. S. Chakraborty**, "Hardware IP Protection During Evaluation Using Embedded Sequential Trojan", *IEEE Design & Test of Computers*, vol. 29, no. 3, Jun. 2012, pp. 70-79.
65. **R. S. Chakraborty** and S. Bhunia, "Security Against Hardware Trojan Attacks Using Key-based Design Obfuscation", *Journal of Electronic Testing: Theory and Applications (Springer)*, vol. 27, no. 6, pp. 767-785, Dec. 2011.
66. **R. S. Chakraborty**, S. Paul, Y. Zhou and S. Bhunia, "Low-Power Hybrid CMOS-NEMS FPGA: Circuit Level Analysis and Defect-Aware Mapping", *IET Computers & Digital Techniques*, vol. 3, no. 6, pp. 609-624, Nov. 2009.
67. **R. S. Chakraborty** and S. Bhunia, "*HARPOON*: A SoC Design Methodology for Hardware Protection through Netlist Level Obfuscation", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 10, pp. 1493-1502, Oct. 2009.
68. **R. S. Chakraborty** and S. Bhunia, "A Study of Asynchronous Design Methodology for Robust CMOS-Nano Hybrid System Design", *ACM Journal of Emerging Technologies in Computing Systems*, vol. 5, no. 3, pp. 1-22, Aug. 2009.
69. **R. S. Chakraborty**, S. Narasimhan and S. Bhunia, "Hybridization of CMOS with CNT-Based Nano Electromechanical Switch for Low Leakage and Robust Circuit Design Using Nanoscaled CMOS Devices", *IEEE Transactions on Circuits and Systems I*, vol. 54, no. 11, pp. 2480-2488, Nov. 2007.

- **Conference Papers/Posters** (in reverse chronological order)

1. **R. S. Chakraborty**, "(Invited paper) PFMPUF: a Configurable and Scalable Ring Oscillator PUF based on Pulse Frequency Modulation", *IEEE Conference on Building a Secure and Empowered Cyberspace (BuildSec)*, Patna, India, 2025.

2. S. Biswas, S. Chakraborty, and **R. S. Chakraborty**, “Redacting Without Regret: A Dual-Layer Framework for Policy-Compliant Blockchains”, *Conference on Blockchain Research & Applications for Innovative Networks and Services (BRAINS)*, Zurich, Switzerland, 2025.
3. A. Dutta, A. K. Das, R. Naskar and **R. S. Chakraborty**, “WaveDIF: Wavelet Sub-band Based Deepfake Identification in the Frequency Domain”, *IEEE Conference on Computer Vision and Pattern Recognition Workshop (CVPRW)*, Nashville, Tennessee, USA, 2025.
4. R. Mukherjee, S. Swaroopa and **R. S. Chakraborty**, “(Invited Paper) Security Vulnerabilities in AI Hardware: Threats and Countermeasures”, *IEEE Asian Test Symposium (ATS)*, Ahmedabad, India 2024.
5. V. S. Balijabudda, I. Chakrabarti and **R. S. Chakraborty**, “Design, Implementation and Characterization of a Novel Robust-by-Construction Arbiter PUF Circuit on Xilinx FPGAs”, *IEEE Asian Test Symposium (ATS)*, Ahmedabad, India 2024.
6. K. Pratihar, S. Chatterjee, **R. S. Chakraborty** and D. Mukhopadhyay, “(Short Paper) Breaching the Gap: Modelling SRAM-PUFs via Side-Channel Signatures”, *ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, Boca Raton, Florida, USA, 2024.
7. A. Bhattacharyya, K. Srijith, R. P. Behera, A. Dasgupta and **R. S. Chakraborty**, “A Study on Effects of Synthetic Data for Predicting the Remaining Useful Life of Aluminium Electrolytic Capacitors Using Bagging-Based Ensemble Learning”, S. Das et al. (eds.), *Proceedings of Advances in Data-Driven Computing and Intelligent Systems (ADCIS)*, Goa, India, 2023.
8. V. S. Balijabudda, K. Acharya, **R. S. Chakraborty** and I. Chakrabarti, “Theoretical Enumeration of Deployable Single-output Strong PUF Instances based on Uniformity and Uniqueness Constraints”, *International Conference on Information Systems Security (ICISS)*, Raipur, India, 2023.
9. Gisha C. G., A. S. Chakraborty, **R. S. Chakraborty**, B. A. Jose, J. Mathew, “Diode-Triode Current Mirror Inverter PUF: A Novel Mixed-Signal Low Power Analog PUF”, *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Phoenix, Arizona, USA, 2023.
10. **[Best Paper Award]** D. Das, R. Naskar and **R. S. Chakraborty**, “Linear and Non-Linear Filter-based Counter-Forensics Against Image Splicing Detection”, *International Conference on Computer Vision & Image Processing (CVIP)*, Nagpur, India, 2022.
11. A. Saha, H. Banerjee, **R. S. Chakraborty** and D. Mukhopadhyay, “Revisiting Logic Obfuscation Using Cellular Automata”, *First Asian Symposium on Cellular Automata Technology (ASCAT)*, Shibpur, India, 2022.
12. A. Saha, U. Chatterjee, D. Mukhopadhyay and **R. S. Chakraborty**, “DIP Learning on CAS-Lock: Using Distinguishing Input Patterns for Attacking Logic Locking”, *Design, Automation and Test in Europe (DATE)*, Antwerp, Belgium, 2022.
13. A. Saha, D. Mukhopadhyay and **R. S. Chakraborty**, “(Extended Abstract) Design and Analysis of Logic Locking Techniques”, *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Singapore, 2021.
14. **[Best Paper Nomination]** P. Santikellur, R. Mukherjee and **R. S. Chakraborty**, “APUF-BNN: An Automated Framework for Efficient Combinational Logic Based Implementation of Arbiter PUF through Binarized Neural Network”, *ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, Virtual Conference, 2021.
15. D. B. Tariang, S. C. Birudaraju, R. Naskar, V. Khare and **R. S. Chakraborty**, “Malware Classification Through Attention Residual Network based Visualization”, *IEEE Asian Hardware Oriented Security and Trust (AsianHOST)*, Kolkata, India, 2020.
16. P. Ghosh, U. J. Botero, F. Ganji, D. Woodard, **R. S. Chakraborty** and D. Forte, “Automated Detection and Localization of Counterfeit Chip Defects by Texture Analysis in Infrared (IR) Domain”, *IEEE International Conference on Physical Assurance and Inspection of Electronics (PAINE)*, Washington, D.C., USA, 2020.

17. U. Chatterjee, R. Sadhukhan, D. Mukhopadhyay, **R. S. Chakraborty**, D. Mahata and M. Prabhu, “Stupify: A Hardware Countermeasure of KRACKs in WPA2 using Physically Unclonable Functions”, *The Web Conference (WWW)*, Taipei, Taiwan, 2020.
18. V. S. Balijabudda, D. Thapar, P. Santikellur, **R. S. Chakraborty** and I. Chakrabarti, "Design of a Chaotic Oscillator based Model Building Attack Resistant Arbiter PUF", *IEEE Asian Hardware Oriented Security and Trust Symposium (AsianHOST)*, Xi'an, P.R. China, 2019.
19. P. Santikellur, Lakshya, S. R. Prakash and **R. S. Chakraborty**, "A Computationally Efficient Tensor Regression Network based Modeling Attack on XOR Arbiter PUF", *IEEE Asian Hardware Oriented Security and Trust Symposium (AsianHOST)*, Xi'an, P.R. China, 2019.
20. S. Chattopadhyay and **R. S. Chakraborty**, “Cyclic Beneš Network based Logic Encryption for Mitigating SAT-Based Attacks”, *IEEE International Conference on Computer Design (ICCD)*, Abu Dhabi, U.A.E., 2019.
21. S. Chattopadhyay, P. Kumari, B. Ray and **R. S. Chakraborty**, “Machine Learning Assisted Accurate Estimation of Usage Duration and Manufacturer for Recycled and Counterfeit Flash Memory Detection”, *IEEE Asian Test Symposium (ATS)*, Kolkata, India, 2019.
22. K. Bagadia, U. Chatterjee, D. B. Roy, D. Mukhopadhyay and **R. S. Chakraborty**, "Revisiting the Security of LPN based RFID Authentication Protocol and Potential Exploits in Hardware Implementations", *International Conference on Security, Privacy and Applied Cryptographic Engineering (SPACE)*, Gandhinagar, India, 2019.
23. V. Govindan, S. Koteswara, A. Das, Keshab K. Parhi and **R. S. Chakraborty**, "ProTro: A Probabilistic Counter based Hardware Trojan Attack on FPGA based MACSec enabled Ethernet Switch", *International Conference on Security, Privacy and Applied Cryptographic Engineering (SPACE)*, Gandhinagar, India, 2019.
24. P. Ghosh, F. Ganji, D. Forte, D. L. Woodard and **R. S. Chakraborty**, “Automated Framework for Unsupervised Counterfeit Integrated Circuit Detection by Physical Inspection”, *IEEE International Conference on Physical Assurance and Inspection of Electronics (PAINE)*, Washington, D.C., USA, 2019.
25. D. B. Tariang, **R. S. Chakraborty**, R. Naskar, A. Roy and P. Sengupta, “Improved Detection and Localization for Copy-move Forgery Detection with Similar but Genuine Objects”, *IEEE Conference on Computer Vision and Pattern Recognition Workshops (CVPRW)*, Long Beach, California, USA, 2019.
26. U. Chatterjee, P. Santikellur, R. Sadhukhan, V. Govindan, D. Mukhopadhyay and **R. S. Chakraborty**, “United We Stand: A Threshold Signature Scheme for Identifying Outliers in PLCs (poster with 2 page short-paper)”, Late Breaking Results (LBR) track of *IEEE/ACM Design Automation Conference (DAC)*, Las Vegas, Nevada, USA, 2019.
27. U. Chatterjee, R. Sadhukhan, V. Govindan, D. Mukhopadhyay, **R. S. Chakraborty**, S. Pati, D. Mahata and M. Prabhu, “PUFSSL: An OpenSSL Extension for PUF based Authentication”, *IEEE International Conference on Digital Signal Processing (DSP)*, Shanghai, China, 2018.
28. P. Ghosh, D. Forte, D. L. Woodard and **R. S. Chakraborty**, “Automated Detection of Pin Defects on Counterfeit Microelectronics”, *International Symposium for Testing and Failure Analysis (ISTFA)*, Phoenix, Arizona, USA, 2018. Co-located with *IEEE International Test Conference (ITC)*, 2018.
29. A. Roy, D. B. Tariang, **R. S. Chakraborty** and R. Naskar, “Discrete Cosine Transform Residual Feature based Filtering Forgery and Splicing Detection in JPEG Images”, *IEEE Conference on Computer Vision and Pattern Recognition Workshops (CVPRW)*, Salt Lake City, Utah, USA, 2018.
30. U. Chatterjee, D. P. Sahoo, D. Mukhopadhyay and **R. S. Chakraborty**, "Trustworthy Proofs for Sensor Data using FPGA based Physically Unclonable Functions", *Design, Automation and Test in Europe (DATE)* 2018, Dresden, Germany.

31. M. Khairallah, R. Sadhukhan, R. Samanta, J. Breier, S. Bhasin, **R. S. Chakraborty**, A. Chattopadhyay and D. Mukhopadhyay, "Differential Fault Attack Resistant Physical Design Automation", *Design, Automation and Test in Europe (DATE)* 2018, Dresden, Germany.
32. D. P. Sahoo, P. H. Nguyen, D. Basu Roy, D. Mukhopadhyay and **R. S. Chakraborty**, "Side Channel Evaluation of PUF-Based Pseudorandom Permutation", *EUROMICRO Digital System Design Conference (DSD)* (special session on Architectures and Hardware for Security Applications), Vienna, Austria, 2017.
33. P. Ghosh and **R. S. Chakraborty**, "Counterfeit IC Detection By Image Texture Analysis (short paper)", *EUROMICRO Digital System Design Conference (DSD)* (special session on Architectures and Hardware for Security Applications), Vienna, Austria, 2017.
34. A. Roy, **R. S. Chakraborty**, U. Sameer and R. Naskar, "Camera Source Identification Using Discrete Cosine Transform Residue Features and Ensemble Classifier", *IEEE Conference on Computer Vision and Pattern Recognition Workshops (CVPRW)*, Honolulu, Hawaii, USA, 2017.
35. A. Roy, A. Konda and **R. S. Chakraborty**, "Copy Move Forgery Detection with Similar but Genuine Objects", *IEEE International Conference on Image Processing (ICIP)*, Beijing, China, 2017.
36. D. B. Tariang, A. Roy, **R. S. Chakraborty** and R. Naskar, "Automated JPEG Forgery Detection with Correlation based Localization", *IEEE International Conference on Multimedia and Expo (ICME)*, Hong Kong, 2017.
37. K. Bagadia, U. Chatterjee, D. Basu Roy, D. Mukhopadhyay and **R. S. Chakraborty**, "Exploiting Safe Error Based Leakage of RFID Authentication Protocol using Hardware Trojan Horse (poster)", *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, McLean, USA, 2017.
38. M. Alam, D. Basu Roy, S. Bhattacharya, V. Govindan, **R. S. Chakraborty** and D. Mukhopadhyay, "SmashClean: A Hardware level mitigation to stack smashing attacks in OpenRISC", *ACM/IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE)*, Kanpur, India, 2016.
39. **[Best Paper Award]** A. Roy and **R. S. Chakraborty**, "Optimal Distortion Estimation for Prediction Error Expansion Based Reversible Watermarking", *International Workshop on Digital-forensics and Watermarking (IWDW)*, Beijing, China, 2016. Published in *Lecture Notes on Computer Science*, vol. 10082, pp. 265-279.
40. Anju P. Johnson, S. Patranabis, **R. S. Chakraborty** and D. Mukhopadhyay, "Remote Dynamic Clock Reconfiguration based Attacks on Internet of Things Applications", *EUROMICRO Digital System Design Conference (DSD)* (special session on Architectures and Hardware for Security Applications), Limassol, Cyprus, 2016.
41. S. Saha, **R. S. Chakraborty** and D. Mukhopadhyay, "Testability based Metric for Hardware Trojan Vulnerability Assessment", *EUROMICRO Digital System Design Conference (DSD)* (special session on Architectures and Hardware for Security Applications), Limassol, Cyprus, 2016.
42. D. P. Sahoo, S. Patranabis, D. Mukhopadhyay and **R. S. Chakraborty**, "Fault Tolerant Implementations of Delay-based Physically Unclonable Functions on FPGA", *Fault Diagnosis and Tolerance in Cryptography (FDTC)* 2016 (co-located with *CHES'16*), Santa Barbara, USA, pp. 87-101.
43. U. Chatterjee, **R. S. Chakraborty**, J. Mathew and D. K. Pradhan, "Memristor based Arbiter PUF: Cryptanalysis Threat and its Mitigation", *International Conference on VLSI Design (VLSID)* 2016, Kolkata, India, pp. 535-540.
44. A. Roy, **R. S. Chakraborty** and R. Naskar, "Reversible Color Image Watermarking in the YCoCg-R Color Space", *International Conference on Information Systems Security (ICISS)* 2015, Kolkata, India. Published in *Lecture Notes on Computer Science* (Springer), vol. 9478, pp. 480-498, 2015.

45. Anju P. Johnson, **R. S. Chakraborty** and D. Mukhopadhyay, "A Novel Attack on a FPGA based True Random Number Generator", *ACM Workshop on Embedded Systems Security (WESS, part of ACM ESWEEK) 2015*, Amsterdam, Netherlands.
46. D. P. Sahoo, **R. S. Chakraborty** and D. Mukhopadhyay, "Towards Ideal Arbiter PUF Design on Xilinx FPGA: a Practitioner's Perspective (short paper)", *EUROMICRO Digital System Design Conference (DSD)* (special session on Architectures and Hardware for Security Applications), Funchal, Portugal, 2015.
47. A. Palchadhuri and **R. S. Chakraborty**, "Automated Design of High Performance Integer Arithmetic Cores on FPGA", *EUROMICRO Digital System Design Conference (DSD)*, Funchal, Portugal, 2015.
48. S. Saha, **R. S. Chakraborty**, S. S. Nuthakki, Anshul and D. Mukhopadhyay, "Improved Test Pattern Generation for Hardware Trojan Detection using Genetic Algorithm and Boolean Satisfiability", *Workshop on Cryptographic Hardware and Embedded Systems (CHES) 2015*, Saint Malo, France. Published in *Lecture Notes in Computer Science*, vol. 9293, pp. 577-596, 2015.
49. P. H. Nguyen, D. P. Sahoo, **R. S. Chakraborty** and D. Mukhopadhyay, "Cryptanalysis of Robust Ring Oscillator PUF with Enhanced Challenge-Response Set", *Design, Automation and Test in Europe (DATE) 2015*, Grenoble, France.
50. A. Palchadhuri and **R. S. Chakraborty**, "Architecture and Design Automation of High Performance Arithmetic Architectures on FPGAs (poster)", *International Conference on VLSI Design (VLSID) 2015*, Bangalore, India.
51. **[Best Poster Award]** A. Palchadhuri and **R. S. Chakraborty**, "High Performance Integer Arithmetic Circuit Design on Reconfigurable Computing Platforms (poster)", *International Conference on High Performance Computing (HiPC) 2014*, Goa, India.
52. Anju P. Johnson, S. Saha, **R. S. Chakraborty**, D. Mukhopadhyay and S. Goren, "Fault Attack on AES via Hardware Trojan Insertion by Dynamic Partial Reconfiguration of FPGA over Ethernet", *ACM Workshop on Embedded Systems Security (WESS, part of ACM ESWEEK) 2014*, New Delhi, India.
53. P. H. Nguyen, D. P. Sahoo, D. Mukhopadhyay and **R. S. Chakraborty**, "Cryptanalysis of Composite PUFs (invited paper)", *International Symposium on VLSI Design and Test (VDATE) 2014*, Coimbatore, India.
54. A. Palchadhuri, **R. S. Chakraborty**, Md. Salman, S. Kardas and D. Mukhopadhyay, "Highly Compact Automated Implementation of Linear CA on FPGAs", *Cellular Automata for Research and Industry (ACRI) 2014*, Krakow, Poland. Published in *Lecture Notes on Computer Science*, vol. 8751, pp. 388-394, 2014.
55. D. P. Sahoo, S. Saha, D. Mukhopadhyay, **R. S. Chakraborty** and H. Kapoor, "Composite PUF: A New Design Paradigm for Physically Unclonable Functions on FPGA", *IEEE International Symposium on Hardware-Oriented Security and Trust (HOST) 2014*, Washington, D.C., USA.
56. R. Naskar and **R. S. Chakraborty**, "On Complexities of Spatial-Domain Reversible Watermarking Algorithms", *International Conference on Computing (INDIACom) 2014*, New Delhi, India.
57. R. Naskar, A. Raju, **R. S. Chakraborty**, "A Single Pass, High Throughput Reversible Watermarking Scheme for Audio based on Redundant Embedding", *International Conference on Signal Processing and Communication (ICSPC) 2013*, Noida, India.
58. D. P. Sahoo, D. Mukhopadhyay and **R. S. Chakraborty**, "Design of Low Area-overhead Ring Oscillator PUF with Large Challenge Space", *International Conference on Reconfigurable Computing and FPGAs (ReConFig) 2013*, Cancun, Mexico.

59. D. P. Sahoo, D. Mukhopadhyay and **R. S. Chakraborty**, “Formal Design of Composite Physically Unclonable Function”, *Security Proofs for Embedded Systems (PROOFS)* 2013, Santa Barbara, California, USA (co-located with *CHES’13*).
60. I. Saha, R. R. Jeldi and **R. S. Chakraborty**, “Model Building attacks on Physically Unclonable Functions using Genetic Programming (short paper)”, *IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)* 2013, Austin, Texas, USA.
61. P. Nagaraju, R. Naskar and **R. S. Chakraborty**, “Improved Histogram Bin Shifting based Reversible Watermarking”, *International Conference on Intelligent System and Signal Processing (ISSP)* 2013, Anand, Gujarat, India.
62. R. Naskar and **R. S. Chakraborty**, “Fuzzy Inference Rule based Reversible Watermarking for Digital Images”, *International Conference on Information Systems Security (ICISS)* 2012, Guwahati, India. Published in *Lecture Notes in Computer Science*, vol. 7671, pp. 149-163, 2012.
63. R. Naskar and **R. S. Chakraborty**, “Lossless Secret Image Sharing based on Generalized–LSB Replacement”, *ACM Research in Applied Computation Symposium (RACS)* 2012, San Antonio, Texas, USA.
64. S. Burman, A. Palchaudhuri, **R. S. Chakraborty**, D. Mukhopadhyay and P. Singh, “Effect of Malicious Hardware Logic on Circuit Reliability”, *International Symposium on VLSI Design and Test (VDAT)* 2012, Shibpur, India. Published in *Lecture Notes in Computer Science*, vol. 7373, pp. 190-197, 2012.
65. R. Naskar and **R. S. Chakraborty**, “Reversible Image Watermarking through Coordinate Logic Operation based Prediction”, *International Conference on Information Systems Security (ICISS)* 2011, Kolkata, India. Published in *Lecture Notes in Computer Science*, vol. 7093, pp. 190-203, 2011.
66. D. Mukhopadhyay and **R. S. Chakraborty**, “Testability of *Cryptographic Hardware* and Detection of *Hardware Trojans* (invited paper)”, *IEEE Asian Test Symposium (ATS)* 2011, New Delhi, India.
67. R. Naskar and **R. S. Chakraborty**, “Lossless Data Hiding for Halftone Color Images”, *International Conference on Image Information Processing (ICIIP)* 2011, Shimla, Himachal Pradesh, India.
68. **R. S. Chakraborty**, S. Narasimhan and S. Bhunia, “Embedded Software Security through Key-based Control Flow Obfuscation”, *International Conference on Security Aspects in Information Technology, High-performance Computing and Networking (InfoSecHiComNet)* 2011, Haldia, West Bengal, India. Published in *Lecture Notes in Computer Science*, vol. 7011, pp. 30-44, 2011.
69. S. Bandyopadhyay, R. Naskar and **R. S. Chakraborty**, “Reversible Watermarking Using Priority Embedding through Repeated Application of *Integer Wavelet Transform*”, *International Conference on Security Aspects in Information Technology, High-performance Computing and Networking (InfoSecHiComNet)* 2011, Haldia, West Bengal, India. Published in *Lecture Notes in Computer Science*, vol. 7011, pp. 45-56, 2011.
70. S. Narasimhan, X. Wang, D. Du, **R. S. Chakraborty** and S. Bhunia, “TeSR: A Robust Temporal Self-Referencing Approach for Hardware Trojan Detection”, *IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)* 2011, San Diego, CA, USA.

71. S. Bandyopadhyay, R. Naskar and **R. S. Chakraborty**, “Reversible Digital Watermarking using Integer Wavelet Transform”, *International Conference on Scientific Paradigm Shift in Information Technology and Management* 2011, Kolkata, India.
72. S. Ali, D. Mukhopadhyay, **R. S. Chakraborty** and S. Bhunia, “Multi-level Attack: an Emerging Threat Model for Cryptographic Hardware”, *Design, Automation and Test in Europe (DATE)* 2011, Grenoble, France.
73. D. Du, S. Narasimhan, **R. S. Chakraborty** and S. Bhunia, “Self-referencing: a Scalable Side-channel Approach for Hardware Trojan Detection”, *Workshop on Cryptographic Hardware and Embedded Systems (CHES)* 2010, Santa Barbara, CA, USA. Published in *Lecture Notes in Computer Science*, vol. 6225, pp. 173-187, 2010.
74. **R. S. Chakraborty**, S. Narasimhan and S. Bhunia, “Embedded Software Security through Key-based Obfuscation (poster)”, *Workshop on Cryptographic Hardware and Embedded Systems (CHES)* 2010, Santa Barbara, CA, USA.
75. **[Best Paper Nomination]** S. Narasimhan, D. Du, **R. S. Chakraborty**, S. Paul, F. Wolff, C. Papachristou, K. Roy and S. Bhunia, “Multiple-parameter Side-channel Analysis: a Non-invasive Hardware Trojan Detection Approach”, *IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)* 2010, Anaheim, CA, USA.
76. S. Narasimhan, S. Paul, **R. S. Chakraborty**, F. Wolff, C. Papachristou, D. J. Weyer and S. Bhunia, “System Level Self-Healing for Parametric Yield and Reliability Improvement under Power Bound”, *NASA/ESA Conference on Adaptive Hardware and Systems (AHS)* 2010, Anaheim, CA, USA.
77. **R. S. Chakraborty** and S. Bhunia, “RTL Hardware IP Protection Using Key-Based Control and Data Flow Obfuscation”, *International Conference on VLSI Design (VLSID)* 2010, Bangalore, India.
78. **R. S. Chakraborty**, S. Narasimhan and S. Bhunia, “Hardware Trojan: Threats and Emerging Solutions (invited paper)”, *IEEE International High Level Design Validation and Test Workshop (HLDVT)* 2009, San Francisco, CA, USA.
79. **R. S. Chakraborty** and S. Bhunia, “Security Against Hardware Trojan Through a Novel Application of Design Obfuscation”, *IEEE/ACM International Conference on Computer-aided Design (ICCAD)* 2009, San Jose, CA, USA.
80. **R. S. Chakraborty**, F. Wolff, S. Paul, C. Papachristou and S. Bhunia: “*MERO*: A Statistical Approach for Hardware Trojan Detection Using Logic Testing”, *Workshop on Cryptographic Hardware and Embedded Systems (CHES)* 2009, Lausanne, Switzerland. Published in *Lecture Notes in Computer Science*, vol. 5747, pp. 396-410, 2009.
81. **R. S. Chakraborty** and S. Bhunia: “Security Through Obscurity: An Approach for Protecting Register Transfer Level Hardware IP”, *IEEE International Workshop on Security and Trust (HOST)* 2009, San Francisco, CA, USA.
82. **R. S. Chakraborty** and S. Bhunia, “Hardware Protection and Authentication Through Netlist-level Obfuscation”, *IEEE/ACM International Conference on Computer-aided Design (ICCAD)* 2008, San Jose, CA, USA.
83. **R. S. Chakraborty**, S. Paul and S. Bhunia, “On-Demand Transparency for Improving Hardware Trojan Detectability”, *IEEE International Workshop on Hardware-Oriented Security and Trust (HOST)* 2008, Anaheim, CA, USA.

84. F. Wolff, S. Bhunia, C. Papachristou and **R. S. Chakraborty**, “Towards Trojan-Free Trusted ICs: Problem Analysis and Detection Scheme”, *Design, Automation and Test in Europe (DATE)* 2008, Munich, Germany.
 85. S. Paul, **R. S. Chakraborty** and S. Bhunia, “VIm-Scan: A Low Overhead Scan Design Approach for Protection of Secret Key in Scan-Based Secure Chips”, *IEEE VLSI Test Symposium (VTS)* 2007, Berkeley, CA, USA.
 86. **R. S. Chakraborty**, S. Paul, and S. Bhunia, “Analysis and Robust Design of Diode-Resistor Based Nanoscale Crossbar PLA Circuits”, *International Conference on VLSI Design (VLSID)* 2008, Hyderabad, India.
 87. S. Paul, **R. S. Chakraborty** and S. Bhunia, “Defect-Aware Configurable Computing in Nano-crossbar Fabric for Improved Yield”, *IEEE International Online Testing Symposium (IOLTS)* 2007, Hersonissos-Heraklion, Crete, Greece.
 88. **R. S. Chakraborty** and S. Bhunia, “Micropipeline-Based Asynchronous Design Methodology for Robust System Design Using Nanoscale Crossbar”, *International Symposium on Quality Electronic Design (ISQED)* 2008, San Jose, CA, USA.
 89. **R. S. Chakraborty**, S. Narasimhan and S. Bhunia, “Hybridization of CMOS with CNT-based Complementary Nano Electro-Mechanical Switch for Low-Leakage and Robust Embedded Memory Design (poster)”, *NSTI Nanotech 2007*, Sunnyvale, CA, USA.
 90. **R. S. Chakraborty** and I. Saha Misra, “A Novel Design Approach for V-Dipole Antennas using Genetic Algorithms”, *International Conference on Antenna Technologies (ICAT)* 2005, Ahmedabad, India.
- **Tutorials and Invited Talks** (in reverse chronological order)
 1. **R. S. Chakraborty**, “AI and Cyber Security: The Double-Edged Sword of Artificial Intelligence”, *AllIoT'25*, Dec. 2025, Kolkata, India.
 2. **R. S. Chakraborty**, “Hardware Security: Threats, Countermeasures, and Opportunities”, *CyberTEA 3.0 Cybersecurity Workshop*, IIT Sri City, Dec. 2025, Chittoor, Andhra Pradesh, India.
 3. **R. S. Chakraborty**, “Differential Cryptanalysis of Cryptographic Permutation and Lightweight Block Cipher through Visualization and Deep Convolutional Neural Network”, *ICSP'25*, NIT Rourkela, Dec. 2025, Rourkela, Odisha.
 4. **R. S. Chakraborty**, “Physical Unclonable Functions (PUFs) and Trusted Hardware Primitives”, *FDP on “Trusted Circuits: Foundations & Frontiers of Hardware Security”*, NIT Rourkela, Dec. 2025, Rourkela, Odisha.
 5. **R. S. Chakraborty**, “[Invited Talk] PFMPUF: a Configurable and Scalable Ring Oscillator PUF based on Pulse Frequency Modulation”, *IEEE BuildSEC'25*, IIT Patna, Dec. 2025, Patna, India.
 6. **R. S. Chakraborty**, “Hardware Security: Threats, Countermeasures, and Opportunities”, *AICTE ATAL FDP on “Introduction to Cyber Security and Ethical Hacking”*, Sikkim Institute of Science and Technology, Oct. 2025, Namchi, Sikkim, India.
 7. **R. S. Chakraborty**, “Large Language Model Assisted Electronic Design Automation: a Paradigm Shift?”, *CCSN'25*, Sep. 2025, Delhi, India.

8. **R. S. Chakraborty**, “Binary Malware and Malicious Network Traffic Detection and Classification using Cryptography and Machine Learning”, *Workshop on Challenges and Best Practices in Threat Detection and Prevention*, Aug. 2025, IIT Kharagpur, India.
9. **R. S. Chakraborty**, “[Invited Talk] Living with AI: Impact on Medicine and Security”, in *Conference on Living with AI: Understanding its Role in Modern Living*, Bengal School of Technology & Management, May, 2024, Kolkata, India.
10. **R. S. Chakraborty**, “[Invited Keynote Talk] Security of the Semiconductor Supply Chain: Threats and Opportunities”, *IC-ETITE’24 Conference*, Vellore Institute of Technology, Feb. 2024, Vellore, India.
11. **R. S. Chakraborty**, “[Invited Panelist in Panel Discussion] Semiconductor in 2026: High Volume and Speed Data: Can current ways of managing security withstand with it?”, *Data Security Council of India Best Practices Meet (DSCI BPM)*, Aug. 2023, Bangalore, India.
12. **R. S. Chakraborty**, “An Overview of State-of-the-art of Secure Computing”, *Summer School of Emerging Technology (Suset)*, Aug. 2023, Haldia Institute of Technology (HIT), Haldia, India.
13. **R. S. Chakraborty**, “Hardware Security: Threats, Countermeasures and Opportunities”, *Invited Talk*, Apr. 2023, Defence Institute of Advanced Technology (DIAT), Pune, India.
14. **R. S. Chakraborty**, “Counterfeit Electronics Detection: Challenge and Electronics”, *Hardware Security Symposium on Emerging Technologies and Their Impact on Civil Society*, Jan. 2023, Amrita Vishwa Vidyapeetham, Coimbatore, India.
15. **R. S. Chakraborty**, “[Plenary Talk] An Overview of State-of-the-art of Secure Computing”, *AICTE Sponsored International Conference on Communication, Computing and Nano-Microwave Technology (CCNMT)*, Jul. 2022, Guru Nanak Institute of Technology, Kolkata, India
16. **R. S. Chakraborty**, “Physically Unclonable Function: a Hardware Security Primitive for IoT Security”, *High End KARYASHALA Workshop on Hardware Assisted Security for Fog Computing based IoT Networks*, Jul. 2022, Dhirubhai Ambani Institute of Information and Communication Technology (DAICT), Gandhinagar, India.
17. **R.S. Chakraborty** and P. Santikellur, “[Tutorial] Modeling Attacks on Physically Unclonable Functions”, *ISEA Virtual Presentation Conclave (IVPC)*, Jun. 2022, IIT Guwahati (virtual event), India.
18. **R. S. Chakraborty**, “Hardware Security: Threats, Countermeasures and Opportunities”, *5th International Conference on Devices, Circuits and Systems (ISDCS)*, Mar. 2022, IEST Shibpur, Howrah, India.
19. **R. S. Chakraborty**, “Can I Trust My Eyes? Introduction to Image Morphing and Digital Image Forensics”, *Online National Computational Intelligence and Blockchain Technology (CIBT)*, Oct. 2021, NIT Raipur, India.
20. **R. S. Chakraborty**, “[Keynote Talk] Can I Trust My Eyes? Introduction to Image Morphing and Digital Image Forensics”, *5th International Conference on Information Systems and Computer Networks (ISCON)*, Oct. 2021, Mathura, India.
21. **R. S. Chakraborty**, “Hardware Security: Threats, Countermeasures and Opportunities”, *Subject-based Webinar Organized by Taylor and Francis*, Jun. 2021, Dr. A. P. J. Abdul Kalam Technical University (AKTU), Lucknow, India.

22. **R.S. Chakraborty** and P. Santikellur, “Deep Learning based Model Building Attack Tool on PUF”, *IEEE Council on Electronic Design Automation (CEDA) organized webinar series titled “CAD for Assurance”*, May. 2021 (virtual event).
23. **R. S. Chakraborty**, “Security Issues in Green IoT”, *AICTE Sponsored Short Term Training Program titled “Green IoT for Green Environment”*, Apr. 2021, Guru Nanak Institute of Technology (virtual event), Kolkata, India.
24. **R.S. Chakraborty** and P. Santikellur, “[Tutorial] Recent Advances in Machine Learning based Modeling Attacks on PUF”, *AICTE Sponsored Short Term Course on “Recent Trends and Applications in Machine Learning”*, Feb. 2021, IEST Shibpur, India.
25. **R. S. Chakraborty**, “Physically Unclonable Function: a Hardware Security Primitive for IoT Security”, *AICTE Sponsored Faculty Development Program on “Internet of Things”*, Jan. 2021, NIT Durgapur, India.
26. **R. S. Chakraborty**, “Counterfeit Electronics Detection: Challenge and Opportunities”, *AICTE Sponsored Short Term Training Program titled “Cyber Security – Current Trends and Future Perspective”*, Dec. 2020, Guru Nanak Institute of Technology (virtual event), Kolkata, India.
27. **R. S. Chakraborty**, “Hardware Trojans: Technology Stack, Instruments, & Strategies”, *Data Security Council of India Annual Information Security Summit (DSCI AISS)*, Dec. 2020 (virtual event), India.
28. **R.S. Chakraborty**, J. Mathew and P. Santikellur, “[Tutorial] Physically Unclonable Functions: Design, Applications and Threats”, *IEEE International Technical Conference of IEEE Region 10 (IEEE TENCON)*, Oct. 2019, Kochi, India.
29. D. J. Forte and **R. S. Chakraborty**, “[Tutorial] Counterfeit Integrated Circuits: Threats, Detection, and Avoidance”, *Cryptographic Hardware and Embedded Systems (CHES)*, Sep. 2018, Amsterdam, The Netherlands.
30. **R. S. Chakraborty**, “Hardware Trojans and Physically Unclonable Functions”, *Hardware Security and Its Applications (HSA)*, Mar. 2018, NIT Durgapur, India.
31. **R. S. Chakraborty**, “Physically Unclonable Function: an Important Hardware Security Primitive”, *Instruction Enhanced Program on IoT for Structural Health Monitoring*, Mar. 2018, IIT Kharagpur, India.
32. **R. S. Chakraborty**, “Counterfeit ICs: Prevention and Detection through Circuit Design and Image Processing”, *IEEE International Symposium on Devices, Circuits and Systems (ISDCS)*, Mar. 2018, IEST Shibpur, India.
33. **R. S. Chakraborty** and P. Mishra, “[Tutorial] Hardware Intellectual Property (IP) Security and Trust: Challenges and Solutions”, *International Conference on VLSI Design (VLSID)*, Jan. 2018, Pune, India.
34. **R. S. Chakraborty**, “Physically Unclonable Function: an Important Hardware Security Primitive”, *Workshop on Applied Security*, Nov. 2017, Scientific Analysis Group (SAG), Defence Research and Development Organisation (DRDO), Delhi, India.
35. **R. S. Chakraborty**, “Hardware Trojans: a Great Threat to National Security”, *Workshop on Applied Security*, Nov. 2017, Scientific Analysis Group (SAG), Defence Research and Development Organisation (DRDO), Delhi, India.
36. **R. S. Chakraborty**, “Research on Digital Image Forensics at SEAL, IIT Kharagpur”, *Cyber Security Awareness Week (CSAW)*, Nov. 2017, IIT Kanpur, India.

37. **R. S. Chakraborty**, “Security in Embedded Systems”, *3rd SERB School on Robotics*, Jun. 2017, IIT Delhi, India.
38. **R. S. Chakraborty**, “[Tutorial] Physically Unclonable Functions”, *GIAN Course on “Internet-of-Things Security: Issues, Innovations and Interplays”*, Dec. 2016, IIT Patna, India.
39. **R. S. Chakraborty**, “Strict Avalanche Criterion and its Implications on PUF Security”, *1st IEEE International Verification and Security Workshop (IVSW)*, Jul. 2016, Sant Feliu de Guixols, Catalunya, Spain.
40. **R. S. Chakraborty**, “Combined Cryptanalysis and Machine Learning based Modeling Attack on LSPUFs”, Special Session on “New Directions in Hardware Security”, *IEEE International Conference on VLSI Design (VLSID)*, Jan. 2016, Kolkata, India.
41. **R. S. Chakraborty**, D. Mukhopadhyay, P. H. Nguyen and D. P. Sahoo, “[Tutorial] Physically Unclonable Function: a Promising Security Primitive for Internet-of-Things”, *IEEE International Conference on VLSI Design (VLSID)*, Jan. 2015, Bangalore, India.
42. **R. S. Chakraborty**, “Physically Unclonable Function: an Important Hardware Security Primitive”, *3rd National Knowledge Network Workshop*, Dec. 2014, Guwahati, India.
43. **R. S. Chakraborty** and P. H. Nguyen, “Lightweight Physically Unclonable Functions: Design and Security Analysis”, *International Conference on Security, Privacy and Applied Cryptography Engineering (SPACE)*, Oct. 2014, Pune, India.
44. **R. S. Chakraborty**, “Hardware Trojans and Physically Unclonable Functions”, *International Conference on Advances in Computing and Communication (ACC)*, Kochi, August 2014.
45. **R. S. Chakraborty** and R. Naskar, “Reversible Watermarking”, *International Conference on Information Systems Security (ICISS)*, Dec. 2012, Guwahati, India.
46. **R. S. Chakraborty**, “[Tutorial] Hardware Trojans: Threats and Emerging Solutions”, *International Conference on Information Systems Security (ICISS)*, Dec. 2011, Kolkata, India.
47. D. Mukhopadhyay and **R. S. Chakraborty**, “[Tutorial] Testability of *Cryptographic Hardware* and Detection of *Hardware Trojans*”, *IEEE Asian Test Symposium (ATS)*, Nov. 2011, New Delhi, India.
48. D. Mukhopadhyay and **R. S. Chakraborty**, “[Tutorial] Information Security from a Hardware Perspective: Challenges and Solutions”, *IEEE International Workshop on Information Security (WIFS)*, Nov. 2011, Foz do Iguacu, Brazil.
49. D. Mukhopadhyay, **R. S. Chakraborty** and C. Rebeiro, “[Tutorial] Hardware Security: a 21st Century Perspective”, *International Conference on VLSI Design (VLSID)*, Jan. 2011, Chennai, India.

- **Patents/Invention Disclosures**

1. A. Dutta, G. Sharma, R. Naskar and **R. S. Chakraborty**, “System for Automatic Malware Detection and Classification Using Image-based Analysis of Binary Files”, Indian patent filed in Aug 2025 (Application No. E-106/2394/2025/KOL).
2. S. Swaroopa, B. V. Sreekanth and **R. S. Chakraborty**, “Method For Run-Time Program Binary Authentication for a Field Programmable Gate Array (FPGA) based Computing Platform To Ensure Secure Binding Of The Program Binary Exclusively to a Specific FPGA

- Platform and a System Thereof”, Indian patent filed in Jan 2025 (Application No. E-2/20/2025/KOL).
3. D. P. Sahoo, D. Mukhopadhyay, P. H. Nguyen and **R. S. Chakraborty**, “A Multiplexer based System for Electronic Device Authentication and Preventing Counterfeiting of the Electronic Device”, Indian Patent #554710, Nov. 2024 (granted).
 4. **R. S. Chakraborty** S. Swaroopa, B. V. Sreekanth and M. Som, “Untrusted Hardware Module Identification and Reporting for Secure System Implementation on Field Programmable Gate Array Platform”, Indian patent filed in November 2024 (Application No. E-11/1070/2024/KOL).
 5. D. Mukhopadhyay, **R. S. Chakraborty**, A. Saha and S. Das, “System for Logic Circuit Obfuscation and Method Thereof”, Indian patent filed in June 2023 (Application No. E-106/488/2023/KOL).
 6. A. Johnson, **R. S. Chakraborty**, D. Mukhopadhyay and C. Irani, “System and Method for Dynamic Partial Reconfiguration of Circuits Mapped or Configured on FPGA Platform”, Indian Patent # 417967, Jan. 2023 (granted).
 7. R. S. Chakraborty, R. Naskar, **B. Sarkar**, “A Method and System for Evaluation of Reversible Watermarking of Digital Images and Audio”, Indian Patent #405072, Aug. 2022 (granted).
 8. J. Mathew, **R. S. Chakraborty**, Y. Yang, A. M. Jabir and D. K. Pradhan, “Circuits and Methods for Memristor based Physically Unclonable Function”, U.S. patent filed in November 2015 (Ref.: Application No. **14948617**).
 9. **R. S. Chakraborty** and A. Palchoudhuri, “Architecture and Design Automation of High Performance Large Adders and Counters on FPGA through Constrained Placement”, International PCT application filed in April 2014 (Ref: PCT/IB2014/060372). Indian Patent filed in February 2014 (Ref: 179/KOL/2014).
 10. **R. S. Chakraborty** and B. K. Diddi, “Multi-level Inline Data Deduplication”, U.S. patent #9,311,323, April 2016 (granted). International PCT application filed in October 2012 (Ref: PCT/IB2012/055688). Indian patent filed in September 2012 (Ref: 1022/KOL/2012).
 11. **R. S. Chakraborty**, S. Narasimhan and S. Bhunia, “Protection of Intellectual Property Cores Through a Design Flow”, U.S. patent #8402401, March 2013 (granted).
 12. **R. S. Chakraborty**, F. Wolff, S. Paul, C. Papachristou and S. Bhunia: “A Statistical Approach to Hardware Trojan Detection using N-Detect Tests and Coverage Estimation using Random Sampling”, Invention Disclosure, Case Western Reserve University, April 2009.

RESEARCH FUNDING

- **Directorate of Futuristic Technology Management (DFTM), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
Project Title: “Secure and Intelligent Indigenous Network Packet Processor on Field Programmable Gate Array with Hardware based Stateful Firewall for Real-time Intrusion Detection/Prevention”
PI: Prof. Rajat Subhra Chakraborty
Co-PI: Prof. Indrajit Chakrabarti
Duration: 3 years (Dec. 2012-Dec.2014)

- **IIT Kharagpur AI4CPS I Hub Foundation**
Project Title: “Malware Executable Detection and Classification through Visualization and Machine Learning”
PI: Prof. Rajat Subhra Chakraborty
Co-PI: Dr. Ruchira Naskar (IEST Shibpur)
Duration: 2 years (Dec 2023 – Dec 2025)
- **IIT Kharagpur AI4CPS I Hub Foundation**
Project Title: “Synthesis of Single Crystal Emerald Using Artificial Intelligence and Hydrothermal Apparatus”
PI: Prof. Sujoy Kanti Ghosh
Co-PI: Prof. Rajat Subhra Chakraborty and Prof. Amreesh Chandra
Duration: 2 years (Feb 2024 – Feb 2026)
- **Intel Corporation**
Project Title: “Security Course Development for Intel Unnati Program”
PI: Prof. Rajat Subhra Chakraborty
Co-PI: Dr. Sandip Chakraborty
Duration: 6 months (Apr 2023 – Sep 2023)
- **Central Power Research Institute (CPRI), Govt. of India**
Project Title: “Cyber Security of Power Systems through Design-for Prevention, Real-time Detection and Effective Intervention”
PI: Prof. Dipanwita Roy Chowdhury
Co-PI: Prof. Pabitra Mitra, Prof. Ashok Pradhan, Dr. Rajat Subhra Chakraborty
Duration: 2 years (Mar 2022 – Mar 2024)
- **Science and Engineering Research Board (SERB), Govt. of India**
Project Title: “A Comprehensive Framework for Adversarial Evaluation of Random Number Generators: Theory and Implementation”
PI: Dr. Rajat Subhra Chakraborty
Duration: 3 years (Jan 2020 – Jan 2023)
- **Intel Corporation**
Project Title: “DeepFake Catcher: Methods to Identify AI Generated Facial Videos and Images”
PI: Dr. Rajat Subhra Chakraborty
Duration: 15 months (Oct 2019 – Jan 2021)
- **Indira Gandhi Centre For Atomic Research (IGCAR), Government of India, Department of Atomic Energy, Govt. of India**
Project Title: “Design and Development of FPGA Implementable Physical Unclonable Function for High Security Authentication Applications”
PI: Dr. Rajat Subhra Chakraborty
Co-PI: Prof. Indrajit Chakrabarti
Duration: 3 years (May 2019 – May 2022)
- **Department of Science and Technology, Govt. of India**
Project Title: “Digital Image Forensics in the Context of a Connected India: Algorithms and Implementation”

- PI:** Dr. Rajat Subhra Chakraborty
Co-PI: Dr. Ruchira Naskar (IEST Shibpur)
Duration: 3 years (Jul 2019 - Mar 2023)
- **Directorate of Futuristic Technology Management (DFTM), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
Project Title: “Secure Resource-Constrained Communication Framework for Tactical Networks Using Physically Unclonable Functions (SeRFPUF)”
PI: Dr. Debdeep Mukhopadhyay
Co-PI: Dr. Rajat Subhra Chakraborty
Duration: 5 years (Jul 2017 - Jul 2022)
 - **Hindustan Aeronautics Limited, Ministry of Defence, Govt. of India**
Project Title: “Design, Implementation & Evaluation of Encryption/Decryption Unit for IFF System”
PI: Dr. Debdeep Mukhopadhyay
Co-PI: Dr. Rajat Subhra Chakraborty
Duration: 2 years (Jan 2017 - Jan 2019)
 - **Intel Corporation (U.S.A.)**
Project Title: “Verification Challenges in Compression and Cryptographic Stacks in *QuickAssist* Technology”
PI: Dr. Rajat Subhra Chakraborty
Duration: 4 years (May 2016 - May 2020)
 - **BRNS, Dept. of Atomic Energy, Govt. of India**
Project Title: “Hardware Security in the Context of a Connected World: Threats and Mitigations”
PI: Dr. Rajat Subhra Chakraborty
Co-PI: Dr. Debdeep Mukhopadhyay
Duration: 3 years (May 2016 - May 2019)
 - **IBM**
Project Title: “Optimize real time encryption performance for high volume storage data traffic by means of software improvements to Linux”
PI: Dr. Rajat Subhra Chakraborty
Duration: 3 years (November 2015 - November 2018)
 - **DEITY, Ministry of Communication and IT, Govt. of India**
Project Title: “Information Security Education and Awareness (ISEA) Project Phase-II”
PI: Dr. Debdeep Mukhopadhyay
Co-PI: Dr. Sandip Chakraborty and Dr. Rajat Subhra Chakraborty
Duration: 5 years (November 2015 - November 2020)
 - **Wipro Limited, India**
Project Title: “Securing Internet-of-Things using Unconventional Cryptographic Techniques”
PI: Dr. Debdeep Mukhopadhyay and Dr. Rajat Subhra Chakraborty
Duration: 4 years (June 2015 - June 2019)

- **Science and Engineering Research Board (SERB), Govt. of India**
Project Title: “High Performance Reversible Watermarking of Digital Images: Theory, Implementation and Impact on Medical Imaging”
PI: Dr. Rajat Subhra Chakraborty
Duration: 3 years (May 2014 - May 2017)
- **Scientific Analysis Group (SAG), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
Project Title: “Power Attacks on Stream Ciphers and Cache Memory Attacks”
PI: Dr. Debdeep Mukhopadhyay
Co-PI: Dr. Rajat Subhra Chakraborty
Duration: 2 years (Mar. 2013 - Mar. 2015)
- **Reconnoiter Technology and Research, India**
Project Title: “Hardware Trojan Attack Testbed on FPGA based Systems” (consultancy project)
PI: Dr. Rajat Subhra Chakraborty
Co-PI: Dr. Debdeep Mukhopadhyay
Duration: 3 years (Dec. 2012 - Dec. 2015)
- **Centre for Artificial Intelligence and Robotics (CAIR), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
Project Title: “Machine Learning based Model-building Attack on PUFs”
PI: Dr. Rajat Subhra Chakraborty
Co-PI: Dr. Debdeep Mukhopadhyay
Duration: 2 years (Dec. 2012-Dec.2014)
- **Centre for Artificial Intelligence and Robotics (CAIR), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
Project Title: “Study of Hardware Malware Vulnerabilities and Mitigation Techniques for FPGAs”
PI: Dr. Rajat Subhra Chakraborty
Co-PI: Dr. Debdeep Mukhopadhyay
Duration: 2 years (Sep. 2010-Aug.2012)
- **Centre for Artificial Intelligence and Robotics (CAIR), Defence Research and Development Organisation, Ministry of Defence, Govt. of India**
Project Title: “Design of Controller for Finite Field Arithmetic on FPGAs” (as co-PI)
PI: Dr. Debdeep Mukhopadhyay
Co-PI: Dr. Rajat Subhra Chakraborty
Duration: 2 years (Oct. 2010-Sep.2012)
- **Sponsored Research and Industrial Consultancy (SRIC), IIT Kharagpur**
Project Title: “Hardware Security: Ensuring TRUST in Integrated Circuits”
PI: Dr. Rajat Subhra Chakraborty
Duration: 2 years (Sep. 2010-Aug.2012)

CURRENT GRADUATE STUDENTS

- **Ph.D.:** B. V. Sreekanth (joint supervisor), Kuheli Pratihar (joint supervisor), M. Sivappriya (joint supervisor), Virendra Kumar Gautam, Astha Agrawal, Shubrojoyoti Karmakar, Abhishek Dutta
- **M.S.:** Anurag Dutta, Pallavi Anand, Sumitava Biswas (joint supervisor)

PAST GRADUATE STUDENTS

- **Ph.D.:**
 - Kuheli Pratihar (2025, supervisor: Prof. Debdeep Mukhopadhyay)
Thesis: “Design and Analysis of Hardware Root of Trust”
 - Rijoy Mukherjee (2025) (currently Staff Engineer at Synopsys)
Thesis: “Security of Domain-Specific Hardware Design: Threats and Mitigations”
 - Akashdeep Saha (2024, supervisor: Prof. Debdeep Mukhopadhyay) – (currently Post-doctoral Researcher at NYU, Abu Dhabi, U.A.E.)
Thesis: “Systematic Design and Efficient Automated Implementation of Secure Logic Locking”
 - Pranesh Santikellur (2022) – (currently Assistant Professor at IIT Bangalore)
Thesis: “Design and Analysis of Machine Learning based Modeling Attacks on Strong Physically Unclonable Functions”
 - Diangarti Bhalang Tariang (2022) – (currently Assistant Professor, NIT Meghalaya, India)
Thesis: “Deep Learning-based Multimedia Forensics and Malware Classification”
 - Urbi Chatterjee (2020, co-supervisor: Prof. Debdeep Mukhopadhyay) – (currently Assistant Professor, IIT Kanpur, India).
Thesis: “Design, Analysis and Implementation of Physically Unclonable Function based Authentication Frameworks for Internet-of-Things”
 - Durga Prasad Sahoo (2017, co-supervisor: Prof. Debdeep Mukhopadhyay) – (currently Sr. Staff R&D Engineer at Synopsys, Bhubaneswar, India)
Thesis: “Design and Analysis of Secure Physically Unclonable Function Compositions”
 - Anju Johnson (2016, co-supervisor: Prof. Debdeep Mukhopadhyay) – (currently Senior Lecturer at University of Huddersfield, U.K.).
Thesis: “Remote Dynamic Partial Reconfiguration for Emerging IoT Applications: Threats and Countermeasures”
 - Ruchira Naskar (2014) – (currently Associate Professor, IEST Shibpur, Howrah, India).
Thesis: “Reversible Watermarking for Digital Images: Algorithms and Implementations”
- **M.S. (through Research):**
 - Sneha Swaroopa (2025)
Thesis: “Hardware Vulnerability Mitigation and Authentication Approaches for Security-sensitive Applications”
 - Vidya Govindan (2019) (currently Senior RTL Design Engineer at Microsoft, Bangalore, India)

- Thesis: “FPGA based Hardware Trojan: Design, Implementation and Detection”
- Pallabi Ghosh (2019) (currently Ph.D. student at University of Florida at Gainesville, U.S.A.)
Thesis: “Counterfeit Integrated Circuit Detection using Image Processing Techniques”
- Aniket Roy (2018) (currently Ph.D. student at Johns Hopkins University, U.S.A.).
Thesis: “Multimedia Security Through Reversible Image Watermarking and Digital Image Forensics”
- Sayandeep Saha (2016, co-supervisor: Debdeep Mukhopadhyay).
Thesis: “Improved ATPG Techniques and Testability Based Metrics for Hardware Trojan Horses”
- Ayan Palchaudhuri (2014) – (currently Assistant Professor, IIT Bhubaneswar).
Thesis: “Architecture and Design Automation of High Performance Integer Arithmetic Soft Cores on Xilinx Field Programmable Gate Arrays”
- Indrasis Saha (2013) – (currently Senior Lead Engineer at Qualcomm, Bangalore, India).
Thesis: “Attacks on FPGA-based System Implementations”.

TEACHING

- **Courses Taught:** Programming and Data Structures (CS11001), Programming and Data Structures Laboratory (CS19001), Switching Circuits and Logic Design (CS21002), Switching Laboratory (CS29002), Systems Programming Laboratory (CS29006), Computer Networks (CS31006), Networks Lab (CS39006/CS49001), Computer Organization and Architecture (CS31007), Computer Organization Laboratory (CS39001), Computer Architecture and Operating System (CS31702), Cryptography and Network Security (CS60065), VLSI System Design (CS60067, IC 80103), High Performance Computer Architecture (CS60003), Hardware Security (CS60004), Performance Modeling of Computer Networks (CS60019), Computing Systems Laboratory (IC89002), M.Tech. Seminar-I (IC89003).

Note: course numbers starting with “6” or higher are PG courses, rest are UG courses.

PROFESSIONAL INVOLVEMENTS

- **Associate Editor:** *Nature Scientific Reports* [Springer] (since 2024), *Cureus Journal of Computer Science* [Springer Nature] (since 2024), *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (2018-2024), *IEEE Transactions on Multi-scale Computing Systems* (till 2018).
- **Publication Co-chair:** *VLSID’24*
- **General Co-chair:** *IEEE AsianHOST’20*
- **Program Co-Chair:** *SPACE’15*, *SPACE’14*, *DSD-AHSA’17*, *DSD-AHSA’20*, *IEEE INDICON’24*
- **Tutorial Co-chair:** *VLSID’18*, *IEEE ATS’19*
- **Member of Expert Panel:** *All India Council for Technical Education (AICTE)* [since 2025]
- **Chair:** IEEE Kharagpur Section (2026)
- **Vice-chair:** IEEE Kharagpur Section (2024)
- **Secretary:** IEEE Kharagpur Section (2023)
- **Treasurer:** IEEE Kharagpur Section (2022)
- **Assistant Secretary:** IEEE Kharagpur Section (2021)
- **Guest Editor:** Special issue on “Secure and Fault Tolerant Embedded Computing” in *ACM Transactions on Embedded Computing Systems* (Sep. 2017)

- **Journal Reviewer:** *Proceedings of the IEEE; IEEE Transactions on Information Forensics and Security; IEEE Transactions on Industrial Informatics; IEEE Transactions on CAD; IEEE Transactions on Dependable and Secure Computing; IEEE Design & Test; IEEE Transactions on Circuits and Systems-I; IEEE Transactions on Circuits and Systems-II; IEEE Transactions on VLSI; IEEE Transactions on Emerging Topics in Computing; IEEE Transactions on Components, Packaging and Manufacturing Technology, IEEE Embedded Systems Letters; ACM Transactions on Design Automation of Electronic Systems; ACM Transactions on Embedded Computing Systems; ACM Journal of Emerging Technologies in Computing Systems; ACM Transactions on Multimedia Computing, Communications and Applications; IET Circuits, Devices and Systems; IET Computers and Digital Techniques; Integration, The VLSI Journal (Elsevier); Digital Signal Processing (Elsevier); Journal of Electronic Testing: Theory and Applications (Springer); Journal of Hardware and Systems Security (Springer); Nature Scientific Reports (Springer); Journal of Supercomputing (Springer)*
- **Book Reviewer:** Book series titled *Synthesis Lectures on Information Security, Privacy, and Trust (Morgan Claypool)*.
- **Academic Judge:** *IEEE E.J. McCluskey Best Doctoral Thesis Award Contest (part of VTS'14), DAC Ph.D. Forum (2017, 2019)*.
- **Program Committee Member:** *IEEE/ACM DAC (2021-), IACR CHES (2021-), IEEE/ACM ICCAD (2022-), IEEE HOST (2018, 2021), IEEE ICCD (2015-2018), IEEE GLSVLSI (2019), RFIDsec (2015), IEEE ISQED (2022-), IEEE AsianHOST (2016-2019), AHSA (part of DSD) (2014-2019), VLSID (2012-2019), VDAT (2012-2014, 2019), IEEE WRTL (2012-2017), ACM RACS (2012), SPACE (2011-), ICISS (2014-), IEEE IVSW (2016-2018), ACM ASHES (2017-2019)*.
- **Other Professional Involvement:** Invited by *IBM* to be part of the *IBM India Onward* initiative, *National Service Scheme (NSS) Program Officer (January 2011 – December 2012)*.

PROFESSIONAL AND ACADEMIC HONORS

- Listed among the top 2% Computer Science researchers in the world (in the “Computer Hardware and Architecture” sub-field), in the “Career-Long” and “Single Calendar Year 2024” categories, as described in the following publication: Ioannidis *et al.*, “August 2025 data-update for "Updated science-wide author databases of standardized citation indicators”, *Elsevier Data Repository*, V8, doi: 10.17632/btchxktzyw.8, Oct. 2025 (available [here](#)).
- Listed among the top 2% Computer Science researchers in the world (in the “Computer Hardware and Architecture” sub-field), in the “Career-Long” and “Single Calendar Year 2023” categories, as described in the following publication: Ioannidis *et al.*, “August 2024 data-update for "Updated science-wide author databases of standardized citation indicators”, *Elsevier Data Repository*, V7, doi: 10.17632/btchxktzyw.7, Oct. 2024 (available [here](#)).
- Listed among the top 2% Computer Science researchers in the world (in the “Computer Hardware and Architecture” sub-field), in the “Single Calendar Year 2022” category, as described in the following publication: Ioannidis *et al.*, “October 2023 data-update for "Updated science-wide author databases of standardized citation indicators”, *Elsevier Data Repository*, V6, doi: 10.17632/btchxktzyw.6, Oct. 2023 (available [here](#)).
- Listed among the top 2% Computer Science researchers in the world (in the “Computer Hardware and Architecture” sub-field), in the “Single Calendar Year 2021” category, as described in the following publication: Ioannidis *et al.*, “September 2022 data-update for “Updated science-wide

author databases of standardized citation indicators”, *Mendeley Data*, vol 4, Oct. 2022 (available [here](#)).

- Listed among the top 2% Computer Science researchers in the world (in the “Computer Hardware and Architecture” sub-field), in the “Single Calendar Year 2020” category, as described in the following publication: Baas *et al.*, “August 2021 data-update for “Updated science-wide author databases of standardized citation indicators””, *Mendeley Data*, vol. 3, Oct. 2021 (available [here](#)).
- Listed among the top 2% Computer Science researchers in the world (in the “Computer Hardware and Architecture” sub-field), in the “Single Calendar Year 2019” category, as described in the following publication: Ioannidis *et al.*, “Updated science-wide author databases of standardized citation indicators”, *PLoS Biology*, 18(10), Oct. 2020 (available [here](#)).
- Recipient of Intel Unrestricted Research Grant Award, 2019.
- Recipient of *Outstanding Faculty Award (Associate Professor level)* from IIT Kharagpur, 2018.
- Recipient of *IEI Young Engineers Award*, 2016.
- Recipient of *Science and Engineering Research Board International Travel Support* grant to attend the *DSD Euromicro Conference* in Limassol, Cyprus, 2016.
- Recipient of *IBM Shared University Research (SUR) Award*, 2015.
- Recipient of *Royal Academy of Engineering (U.K.) Research Exchange Fellowship* award, 2014.
- Recipient of *Microsoft Research India Unrestricted Research Grant* of Rs. 100,000, 2013.
- Recipient of *Council of Scientific and Industrial Research International Travel Support* grant to attend the *RECONFIG* conference in Cancun, Mexico, 2013.
- Recipient of *IBM Faculty Award*, 2012.
- Recipient of *Department of Science and Technology International Travel Support* grant to attend the *IEEE WRTL* workshop in Niigata, Japan, 2012.
- Invited to deliver a plenary session keynote talk on *Testing Techniques for Hardware Trojan Detection* in the *IEEE WRTL* workshop in Niigata, Japan, 2012.
- Semi-finalist in the *IEEE E.J. McCluskey Best Doctoral Thesis Award Contest*, and invited to present (as part of the contest) at the *28th VLSI Test Symposium (VTS)* at Santa Cruz, CA, U.S.A., 2010.
- Recipient of *DAC Young Student Support Program (YSSP)* travel and attendance grant, awarded by ACM and IEEE, to attend the *46th Design Automation Conference (DAC)* at San Francisco, CA, U.S.A., 2009.
- Selected to present at the *ACM/SIGDA Ph.D Forum* at the *46th Design Automation Conference (DAC)* at San Francisco, CA, U.S.A., 2009.
- Recipient of the *Ruth Barber Moon Award for academic excellence and leadership promise* from the School of Graduate Studies, Case Western Reserve University, 2009.
- Recipient of the *Verhosek Fund Graduate Travel Assistance Award* from the Graduate Student Senate of Case Western Reserve University, 2009.
- Recipient of *Graduate Research Fellowship* (including full tuition waiver), Dept. of EECS, Case Western Reserve University, 2006-2007.
- Recipient of *Research Assistantship* (including full tuition waiver), Dept. of EECS, Case Western Reserve University, 2007-2010.

- Felicitated by the *Telegraph Education Foundation*, for securing the 10th Rank in the WBJEE (engineering entrance) examination, 2001, and 17th Rank in the Higher Secondary (12th Standard) Examination in the state, 2001 (out of approx. 40,000 candidates).
- Felicitated by Govt. of West Bengal, India, for securing the 17th Rank in the Higher Secondary (12th Standard) Examination in the state, 2001 (out of approx. 400,000 candidates).

PROFESSIONAL MEMBERSHIP

- Senior Member, IEEE
- Senior Member, ACM

OTHER INFORMATION

- Nationality: Indian
- Year of Birth: 1982
- Gender: Male (He/Him/His)
- Married, with one daughter.